ScR PROTOCOL CONVERTER

TECHNICAL MANUAL

Variation 0

Version 0

SIGHTHILL SMA

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SECTION 1 - DESCRIPTION

Introduction

The ScR Protocol Converter is intended for use as a serial transmissions buffer between any two systems which, athough required to communicate, use incompatable transmission protocols on their serial I/O links. It consists of a standard 3U 19" rack housing, in addition to the necessary power supply and connectors, a processing card (ScR Line Routeing card) and two modems.

Operation

The ScR Protocol Converter is inserted in the serial link between the two systems and operates by intercepting messages from either system and re-transmitting them, using the correct protocol, to the other. It is consequently transparent in use. Each system appears, at its own interface, to be communicating with the other using its own protocol.

To ensure this transparency the PC must operate at such a speed as to enable each system to receive the anticipated response within whatever window is allowed by its own protocol. Should the protocols be message based, the processing card will delay retransmission until this high level protocol is satisfied.

Each of the modems in the PC is dedicated to a single serial link (over which the PC communicates with one of the systems) and is connected to the LR card through a RS232 link. Each link connects with one of the two UARTs on the LR card.

These UARTs are both controlled by the card's on-board micro-controller (an 8748 series device) and, in accordance with pre-programmed instructions from the micro-controller, handle the first level protocol (framing, parity etc.) for the connected link.

The protocol conversion as such is carried out by the micro-controller, which runs a programme written specifically for the application. This programme initialises each of the UARTs to use the message format of the system connected to the serial link served by that UART and, on receiving an incoming message from either system, strips the protocol from the message, reformats it in the protocol of the other system, and forwards the message (now in the correct protocol) to the other system.

With the appropriate programme, the microcontroller can also filter incoming messages; retransmitting only those of concern to the other system. In these circumstances any acknowledgment required by the originating system protocol would be generated by the microcontroller.

Operating Parameters-

Base System

The system is intended for FSK use over VF links operating at up to 1200 Baud. The transmission/reception rate for each of the four channels can be selected individually (by links on the Line Routeing card). These links allow any combination of standard Baud rates in the range 75 - 2400 to be selected; however the links allow only two distinct Baud rates to be used in a given configuration, and the modems chosen limit the maximum baud rate to 1200.

The transmission/reception standard used on each of the serial links is determined individually by the internal wiring of the PC: specifically, by wire-wrapping on the modem edge connectors which determines the operating mode of each modem.

Transmission Levels

The level of the transmitted signals can be varied over two ranges using a pre-set on each modem card.

High Range: between 0dBm and -14dBm
Low Range: between -14dBm and -28dBm

The range is selected by a link on the modem PCB.

Receiver Threshold

The sensitivity of the receiving modem can be chosen to be either -40dBm or -50dBm using a link on the modem card.

Alterations to the Parameters

The modem can cater for a variety of operating standards, however each will require an alteration to the internal wiring of the PC rack since selection is by backplane wiring (see CARDS - MODEM).

Since a change of application, involving changes to transmission standards and/or protocols, would doubtless require reprogramming of the micro-controller and/or reconfiguration of the hardware; such changes should be regarded as the creation of a new EVARIATIONF of the PC.

Changes of a minor nature to an existing variation should be regarded as generating a new VERSION of that variation.--

Reference Variation- (Variation 0)
Reference Version- (Version 0)

Summary

Variation 0:

Link 1 Protocol - BR1810
Link 2 Protocol - ScR3
Line configuration - 4 wire, Full Duplex
Cards: ScR Line Routeing card (90SES3), ScR MODEM (89SES2)

Version 0:

Software - PCLR8749 13/05/92
Link 1 Baud Rate (send & receive): 1200
Link 2 Baud Rate (send & receive): 1200
Power Source: 110V AC
Power Supply: Vero PK55
Line connection: by 15w 'D', transmit pins 3&11, receive pins 1&9

Exegesis

Intended Application - Vaughan TD to Plessey SMA

The communication standard is 4-wire full duplex 1200 Baud; specifically CCITT V23 M2 FULL DUPLEX. The modem configuration used and the internal wiring of the frame have been determined by the requirements of this standard. The Line Routeing card links have been set to give 1200 Baud Tx and Rx clock rates on both UARTs.

Communication between the TD and the PC uses BR1810 protocol.
Cummunication between the PC and the SMA uses ScR3 protocol.

The output from the TD uses a facility provided for ATR purposes (channel 14). The berths intended for SMA use have been designated as ATR reporting points within the TD and generate messages appropriate to this use. When each message is received by the PC, the PC generates the expected Acknowledge message. It then reconfigures the message in the ScR3 protocol and transmits it to the SMA. Normally, the PC will receive an Acknowledge message from the SMA.

Should no Ak be forthcoming from the SMA, the PC will attempt to transmit the message twice more before assuming the link to have failed. When the link fails the PC will output (to the SMA) "Time Request" messages at regular intervals until a "Time" message is received. On receipt of "Time", the PC will Ak the message and assume the link to be functional.

Exegesis (cont.)

This "Time Request" is also transmitted to the SMA whenever the PC becomes operational following power-up or reset. It is not used in this application other than to establish that the link is functional. Normally the SMA would expect to receive a dump of the contents of all designated SMA berths in response to the "Time" message, however, since the ATR channel is not equipped to generate such a response, "Time" is dealt with solely by the PC and the simple AK transmitted is taken by the SMA as an "All Berths Empty" return.

The main direction of transmission between PC and TD is from the TD: transmission from the PC being limited to the appropriate AK messages. Failure of this link will be detected by the TD and indicated by its failure to receive the correct AK message. In these circumstances the TD will declare the link failed and continuously output a test message to the PC. The fault will be assumed to have cleared when a valid AK is received.

Should a transmission error be detected by either of the UARTs, the microcontroller will turn on one of the two yellow LEDs on the front of the LR card. Each of these is dedicated to a particular link. The subsequent receipt of a valid message on the link will cause the microcontroller to extinquish the LED. No other LEDs on the LR card are used in this application.

2 - FAULT INVESTIGATION

Introduction

The important point to grasp when investigating a fault in this system is that the main function, protocol conversion, is confined to the Line Routeing card. The system consists of this card, two MODEMs (one to allow the card to communicate with the TD, one to allow the card to communicate with the SMA), and a power supply. Hence three modes of failure are possible:

Power Failure

Transmission Failure

Computing Failure

Power Failure

As usual, fault finding on this system should begin by eliminating the first of these modes - not on the grounds of probability but because fault investigation of the other modes relies on the integrity of the power supplies.

Even in the absence of black smoke and strange burning smells, a power fault should be easily identified. The presence of each of the three DC voltages used is indicated by a LED on the faceplate of the PS module. If the LED is lit, the voltage -should- be present. However, the LED is only a rough indication and the voltage may be outwith the operating range of the cards in the system. To be certain, the voltages should be checked on the bus-bar (this is particularly important in the case of the 5V supply). Adjustment is possible using potentiometers built into the faceplate.

If none of the LEDs are lit, check that the 110V supply is present. The supply to the PC is from the same source as the supply to the TD. If the TD is working, check the fuse on the rear of the PC rack.

A spare power supply module should be available in the event of the fitted module proving to be faulty. The module simply plugs into the rack and can be changed with ease after loosening the two securing screws. Before fitting a new module or replacing a blown fuse, remove all cards from the frame. If possible, each of the DC busbars should be checked for obvious short circuits with the cards out and then with the cards replaced one by one. (The power supply fault may have been caused by a fault on one of the cards, and this procedure should prevent the replacement from being damaged in a similar manner). As an additional guide, it is worth noting that the supplies fitted have protected outputs which will "crowbar" if presented with a short circuit, and that this condition can usually be detected by the presence of a "whistling" noise.

Transmission Failure

Beyond the LR card, we are, in essence, simply dealing with standard transmission arrangements. Faults on the transmission links will respond to the normal techniques with the additional help that the ScR MODEMs carry extensive diagnostic information in the form of LED indications on the card edge. The use of these LEDs forms the basis of the following procedures, but in addition it is necessary to know how to force transmission from the three systems involved.

Forcing Transmission

On power-up following a "Reset" the PC will transmit a "Time Request" message to the SMA which will respond with an acknowledgement and a "Time Reply" message. The PC will respond to a valid "Time Reply" with an acknowledge sent to the SMA.

The TD will transmit to the PC when one of the designated SMA berths (which are listed elsewhere) becomes occupied. The PC will respond to a valid message from the TD with an acknowledge.

Hence, to force communication between PC and SMA: reset the PC. This is achieved by removing power from the LR card for a few seconds, for which the easiest method is to turn the key/switch which controls the 110V supply.

To force communication between the TD and the PC: interpose a test description into one of the designated berths.

You will have noticed that two-way communication depends on the original message being seen as valid by the receiving system: this will be dealt with under "Computing Faults".

The five LEDs are:

RTS - This LED indicates the condition of a control signal required to enable the MODEM for transmission.

DTR - This LED indicates the condition of a control signal required to enable the MODEM to output received data.

TxD - This LED is lit whenever the TxD input is at binary 0. During normal operation of the MODEM this LED should appear to vary in intensity as it follows the binary value of the transmitted data. When no transmission is occuring this LED is not lit.

Transmission Failure- (cont.)

CD - This LED is lit whenever the MODEM detects the carrier frequency to be present at a signal strength sufficient to guarantee the integrity of the received data. The carrier should be present whether the link is in use or not, and hence this LED should be continuously lit.

RxD - This LED is lit whenever the RxD output is at binary 0. During normal operation of the MODEM this LED should appear to vary in intensity as it follows the binary value of the received data. When no incoming messages are present this LED is not lit.

RTS, DTR and TxD each merely indicate the condition of an external input after passing through a single buffer stage of the MODEM.

In this application the inputs to RTS and DTR are hardwired on the backplane edge-connector and are of limited value in detecting the presence of MODEM faults. If either of these LEDs is not lit, and if, after changing the MODEM, those of the replacement are not lit, a backplane wiring fault is likely to have developed and the fault should be classified as second line.

TxD conveys rather more information, specifically, that data from the LR card is reaching the MODEM. If this LED flashes when the PC is required to transmit, test the lines using an earpiece. If a strong carrier is present, and if it can be heard to modulate when the PC transmits, the fault is likely to be external to the system. If the carrier is not present check that the Line Protection Block fuses are intact, and if so change the MODEM. If the carrier is present but does not modulate, change the MODEM.

If TxD does not flash when the PC is required to transmit, the balance of probabilities is that the fault is either in the LR card or the backplane wiring; however, try changing the MODEM first before treating the fault as a computing fault.

CD and RxD are considerably more informative about the condition of the MODEM and other transmission equipment.

If CD is not lit, either the lines or the remote MODEM may be at fault. Test the lines using an earpiece. If the incoming signal is strong and the Line Protection Block fuses are intact, the MODEM should be changed.

If RxD is not lit (with CD lit) when the SMA is transmitting, the fault is probably at the remote end. However, if the earpiece shows the carrier to be being modulated, the MODEM should be changed.

Transmission Failure- (cont.)

If RxD shows incoming data when the SMA is transmitting, change the MODEM first, since there remains a buffer stage of the MODEM following the indication and a MODEM fault remains a possibility. However the probability is that data is leaving the MODEM and a LR card or backplane wiring fault is much more likely. If changing the MODEM has no effect (as is likely) treat the fault as a computing fault.

All the above assumes that the transmission power supply is present at both MODEM and LR card.

Computing Failure

I know this is rather a vague term. I use it here to cover faults involving those aspects of the system which operate beyond the level of the purely physical communication paths between the PC and the systems to which it interfaces. Before considering a fault of this kind, any suspicion of a power supply or transmission fault should, as far as possible, be eliminated.

You will be led to suspect a computing fault if, whilst exploring the possibility of a transmission fault, you discover one of the following conditions:

1) The PC fails to acknowledge transmissions from the TD although RxD flashes and the MODEM is not at fault.

2) The PC accepts transmissions from the TD but does not transmit to the SMA.

3) The PC does not transmit to the SMA following Reset and the MODEM is not at fault.

4) The PC continuously transmits to the SMA at 10 second intervals.

Conditions 2 & 3 can be confidently assigned to a fault in the PC, but conditions 1 & 4 may be due either to the PC or to the TD and SMA respectively.

In condition 1, either the TD is transmitting invalid messages or the PC is interpreting valid messages as invalid and rejecting them.

In condition 4, the SMA may be failing to respond to valid transmissions from the PC or the PC is either transmitting invalid messages to the SMA or rejecting messages from the SMA as invalid.

The Line Routeing card has LED indications on the card edge which, although not extensive, may be of help in determining where the fault lies in conditions 1 & 4. These are:

The two yellow LEDs, which indicate that transmission errors have been detected on the links:
LED 1 for Link 1, LED 2 for Link 2.

For Sighthill, the link to the TD is link 1 and that to the SMA is link 2.

NOTE: LED 1 is the lower of the two yellow LEDs.

Computing Failure (cont.)

These LEDs are lit on power-up and will extinguish only when error-free messages have been received on their respective links.

The LEDs are controlled by the processor on the basis of a status report read at intervals from the UART. Once the LEDs have been extinguished by correctly received messages, they will light only when the UART status report indicates that an error has been detected in an incoming message. (It should be noted here that the LEDs give no indication as to the validity of the outgoing messages.)

Thus if, under condition 1, LED 1 is lit and messages are arriving from the TD, the LR card is rejecting the messages as invalid.

If, under condition 4, LED 2 is lit and messages are being received from the SMA, the LR card is rejecting the messages as invalid.

Once convinced, under any of the four conditions, that the fault lies with the PC, the only course is to replace the LR card. If the fault then persists, the fault is second line.

The LR card edge actually carries five diagnostic LEDs in addition to the two yellow LEDs:

Three green LEDs indicate which Rx source is being routed to the Rx output. These are labelled (from the top) RX1, RX2 and RX3.

Two red LEDs indicate whether either link has been put into loop-back mode. These are labelled (from the top) L1 and L2.

Since neither the loop-back facility nor the Rx output is used by the PC, none of these five LEDs should be lit in a properly functioning PC system. If any is/are lit, the LR card is faulty and should be replaced.

SECTION 3 - CARDS

Introduction

This section is intended for reference and to satisfy the advanced curiosity: the treatment of the cards covers all areas of circuitry whether used in this application or not. The reader interested only in the general function of the cards in this application should refer to the DESCRIPTION section.

Line Routeing Card - 90SES3- (see drawing)

The Line routeing card is an intelligent card for controlling the routeing of V24 data signals.

There are four main circuit elements:

1) A circuit routeing a single V24 data source (TXRR) to three transmitters.

One Transmitter (L3TX) is permanently enabled, this is intended as a local repeat facility for the source. The two remaining Transmitters (L1TX, L2TX) can be individually enabled or disabled by the processor (these transmitters are intended for connection to line).

In addition, data can be routed to the line transmitters from sources other than TXRR, namely the Rx circuits (loopback mode) or the UARTs (see below). Whichever source is connected, a "break" condition can be forced on either line Transmitter by the processor.

2) A circuit routeing data from three V24 data sources (L1RX, L2RX, EL3RX) to a single Transmitter (RXRR).

One source (L3RX) is intended for local connection, the two others (L1RX, L2RX) for line connection. Whichever Receiver is enabled, a "break" condition can be forced on the (RXRR) Transmitter by the processor.

3) An 8748 series microprocessor controlling two UART's

The microprocessor can transmit or receive via either of the two UART's.

One UART is committed to line 1 of the Transmit and Receive circuits (see above) the other to line 2.

The intention is that the Micro-processor should monitor transmissions received by the UART's and route data, based on a predetermined strategy. To this end, Port 1 of the Micro-processor can read codes preset on two 8 bit DIL switches and thus determine the operating conditions.

Interrupts connected between RxRDY on each of the UART's and the interrupt pin of the Micro-processor, in combination with direct presentation of the two RxRDY signals at one of the Micro-processor expansion ports, allow the Micro-processor to respond rapidly to received data.

Line Routeing Card - 90SES3 (cont.)

When used for transmission, TxRDY on each of the UART's can be tested via an expander port of the Micro-processor.

Provision has been made for parallel off-board communication by the Micro-processor.

Three bi-directional buses are provided.

I) A 4 bit expander port (Directly available at the edge connector).

II) The 8 bits of port 1 are available (via a transparent buffer) at the edge connector - provided only one of the DIL switches (see above) is in use.

III) The main data bus is available at the edge connector via a socketed buffer position capable of taking latching/transparent buffers (eg. '646). The buffer control pins can be operated either by the Micro-processor or external circuits. To facilitate use of the buffer the bus RD/WR pulses are available on the edge connector in a maskable form together with their inverts. Provision has also been made for masking external BRD/BWR pulses and the masked pulses (ENG1/ENG2) are available on the edge connector together with their inverts. Two testable inputs of the Micro-processor, (T0 and T1) are available at the edge connector should they be required for use in handshaking.

Additionally two optically isolated inputs can be tested via one of the Micro-processor ports.

4) A Bit Rate Generator

Five Baud rate clocks (2400, 1200, 600, 300, & 75) are available for use with the UARTs (however only two can be used on-board at any one time). The Tx/Rx rates of the UART's can be independently selected.

The clocks which determine these Baud rates are derived from a bit rate generator with 16 output frequencies. Any two of these frequencies (selected by on-board links) can be made available at the edge connector at all times for use with other cards (eg. the ScR ASAD).

Line Routeing Card - 90SES3 (cont.)

Indications

Seven LED's are provided on the leading edge of the board as a guide to the operational status of the above circuits.

The three green LEDs indicate which Rx source is being routed to the Rx output.

The two red LEDs indicate if either line has been put into loopback mode.

The two yellow LEDs are controlled via the backplane, from where one can be driven via an inverting buffer and the other via either an inverting or non-inverting buffer (link selectable) for application specific indication requirements.

The inputs to these two LED's double as testable inputs for Expander 1, port 4, bits 2 and 3.

Line Routeing Card - 90SES3 (cont.)

Control Signals

The microprocessor controls the operation of all input or output circuits (including Tx/Rx) through its expansion ports. These are allocated as follows:-

Expander 1

P4 0 - Test for opto isolator 1 input
P4 1 - Test for opto isolator 2 input
P4 2 - Testable input LED 1
P4 3 - Testable input LED 2

P5 0 - Tests for UART 1 TxRDY
P5 1 - Tests for UART 2 TxRDY
P5 2 - Tests for UART 1 RxRDY
P5 3 - Tests for UART 2 RxRDY

P6 Bits 0-2 set buffer operating modes latching/transparent.
Bit 3 is NORed with the UART 1 RxRDY interrupt.

P7 Available at edge connector

Expander 2

P4 - 0 Gates TXRR data to line 1 Tx
P4 - 1 Gates TXRR data to line 2 Tx
P4 - 2 Gates line 1 Rx data to line 1 Tx
P4 - 3 Gates line 2 Rx data to line 2 Tx

P6 - 0 Gates line 1 Rx data to RXRR
P6 - 1 Gates line 2 Rx data to RXRR
P6 - 2 Gates line 3 Rx data (local) to RXRR
P6 - 3 is NORed with the UART 2 RxRDY interrupt.

P5 - 0 Gates UART 1 Tx data to line 1 Tx
P5 - 1 Gates UART 2 Tx data to line 2 Tx
P5 - 2 Selects DIL Sw 1 to port 1
P5 - 3 Selects DIL Sw 2 (or external port 1 if all switches open) to port 1

P7 - 0 Forces "break" on line 1 Tx
P7 - 1 Forces "break" on line 2 Tx
P7 - 2 Forces "break" on RXRR
P7 - 3 Selects mode (input or output) of SW 2 buffer

Line Routeing Card - 90SES3 (cont.)

Edge Connector allocation

c		a
0V	1	0v
LED2/PSEN	2	RESET\
VCC	3	VCC
L1TX	4	L1RX
L2TX	5	Rx a
L3TX	6	L3RX
TXRR	7	-12V
V24 RET	8	V24 RET
RXRR	9	+12V
CBA	10	G\
CAB	11	EDIR
ENG2	12	ENG1
G2	13	G1
WR\	14	RD\
WR	15	RD
GEN\	16	LED1
D0	17	D1
D2	18	D3
D4	19	D5
D6	20	D7
T0	21	T1
P7B0	22	P7B1
P7B2	23	P7B3
P1B0	24	P1B1
P1B2	25	P1B3
P1B4	26	P1B5
P1B6	27	P1B7
I1	28	I2
ENG2\	29	ENG1\
O1	30	ALE
CK	31	XCK
VISO RET	32	VISO

c	a

ScR V21/V23 Modem - (89SES2)

The ScR V21/V23 modem consists of a single printed circuit board with indications for Transmitted Data, Received Data, Request To Send, Data Terminal Ready, and Carrier Detect. All connections are made via the DIN 41612 a & c edge connector.

The modem is a combined Frequency Shift Keyed (FSK) Transmitter and Receiver complying with British Standards BS6301, BS6304, BS6328 and CCITT recommendations V21 and V23. It can operate at 300 baud 2-wire full duplex, and 600 or 1200 baud half duplex. It can also operate in loopback mode giving 1200 baud 4-wire full duplex. The mode of operation is set by wire wrap links on the DIN 41612 edge connector.

The data interface can be either TTL/Cmos compatible or V24 (RS232).

The TTL/Cmos interface has inputs capable of working from either TTL or Cmos logic levels and Outputs which can be set to either 5V or 12V Levels by link selection (LK5). Both non-inverted and inverted outputs are provided.

The transmitter output signal can be adjusted over the range of -28 to 0dBm by means of a link (LK1) and preset. The output impedance is 600 ohms and can be isolated through a transformer by link selection (LK3). This output can also be used to form part of an active hybrid allowing 2-wire line connection.

The receiver input is high impedance but an on-board 600 ohm resistor can be used to terminate the line. A transformer is provided for isolation. Both resistor and transformer are link selectable (LK4). The input sensitivity can be set to -40 or -50dBm by a link (LK2).

The modem operates from a 12V DC or AC supply.

ScR V21/V23 Modem - (89SES2)

Electrical characteristics

Power

DC input voltage 12V +/- 10%
AC input voltage 12V +/- 10%
Consumption 6 Watts

Supply current (V24) 130mA
Supply current (TTL/Cmos) 90mA

Data Interface

TTL/Cmos input current -10 to +10 uA
TTL/Cmos input logic 1 1.5 to 30V
TTL/Cmos input logic 0 -0.5 to 1V
TTL/Cmos output sink
Vl = 0.5V
Non-inverted output 16mA
Inverted output 2mA
TTL/Cmos output source
Vh = 5/12V - 1V
Non-inverted output 0.1mA
Inverted output 2mA

V24/28 complies with CCITT

Transmitter

Modulation FSK
Transmit level (V23) -28dBm to 0dBm
Transmit level (V21) -1dBm to -15dBm
Output impedance 600 ohms +/-10%

Receiver

Carrier detect threshold
standard sensitivity -40dBm
high sensitivity -50dBm

Input impedance (high) 100K ohms
Input impedance (low) 600 ohms

Misc.
Line transformer isolation 3.54KV rms or 5KV DC
Temperature range 0 degrees C to 50 degrees C

ScR V21/V23 Modem - (89SES2)

Configuration

Configuration is achieved by wire wrap links on the DIN 41612 connector and by links on the printed circuit board.

Communication modes

(0 indicates that the pin should be wrapped to a11)

Edge connector pin	a12	c12	a13	c13	a14
CCITT V21 Orig. 300 bps full duplex	0	0		0	0
CCITT V21 Ans. 300 bps full duplex		0		0	0
CCITT V23 Mode 2 1200 bps half duplex	0			0	0
CCITT V23 Mode 2 with equalizer 1200 bps half duplex				0	0
CCITT V23 Mode 1 600 bps half duplex	0	0	0		0
CCITT V21 Orig. loopback	0	0		0	
CCITT V21 Ans. loopback		0		0	
CCITT V23 Mode 2 Main loopback	0			0	
CCITT V23 Mode 2 with equalizer loopback				0	
CCITT V23 Mode 1 Main loopback	0	0	0		
CCITT V23 Back loopback	0	0			

Links

LK1 - Out: Transmitter output adjustable -28dBm to -14dBm
In: Transmitter output adjustable -14dBm to 0dBm

LK2 - Out: Receiver input sensitivity -40dBm
In: Receiver input sensitivity -50dBm

V23 operation -

LK3 In
LK4 1 & 2 In: 600 ohm input impedance
LK4 2 & 3 In: 600 ohm input impedance (isolated)
LK4 Out: 100K ohm input impedance

V21 operation -

LK3 In
LK4 Out
Wrap a8 to a7E

ScR V21/V23 Modem - (89SES2)

TTL/CMos configuration

V24 - B9 & B10, MC1488
LK5 3 & 4 In

TTL/CMos - B9 & B10, 74C00
LK5 5 & 6, 7 & 8 In
LK5 1 & 2 In for 5V output
LK5 3 & 4 In for 12V output
Remove D1 & D2

ScR V21/V23 Modem - (89SES2)

Edge Connector allocation

c		a
	1	
	2	
Tx b	3	Tx a
	4	
Rx b	5	Rx a
	6	
600R Termination	7	Rx In
	8	Hybrid o/p
Hybrid i/o	9	Tx o/p Hi Imp.
	10	
10V out	11	5V out
MC1	12	MC0
MC3	13	MC2
DTR TTL	14	MC4
RTS TTL	15	BRTS TTL
CTS TTL	16	BCTS TTL
TxD TTL	17	BTxD TTL
CD TTL	18	BCD TTL
RxD TTL	19	BRxD TTL
BRTS V24	20	DTR V24
Spare Inverter Out	21	Spare Inverter In
	22	BRxD V24
BCTS V24	23	BTxD V24
	24	BCD V24
	25	
0V	26	CD V24
CTS V24	27	DSR V24
RxD V24	28	RTS V24
0V	29	TxD V24
AC	30	
AC	31	+12V In
0V	32	0V

c	a

SECTION 4 - SOFTWARE

SIGHTHILL TRAIN DESCRIBER - BERTH IRN'S

BERTH	IRN
S093	53D
S092	52D
S065	51D
S032	50D

NOTE: No separate berth for S075

GENERAL NOTES

At power up LED1 and LED2 are lit, SMALNK set at fail, and Time Request message (Stx FF Etx FC) sent to SMA at 10sec intervals

When SMA responds with ACK and Time Reply (Stx Hr Mn Sc Etx BCC) then ACK sent to SMA and SMALNK set OK
First message to SMA consists of "Stx 00 n d1 d2 d3 Etx BCC" then changes to "Stx 80 n d1 d2 d3 Etx BCC"
Change to Base Scan (00) for one message every time Time Reply received

If data byte received with error detected then LED1 (TD) or LED2 (SMA) is lit until a data byte is received error free on the corresponding link

TD messages which are CA or CB or CC type have headers viz:-
"Soh T R P S T R A H Stx 0 C C S 0 9 3 4 E 4 4 1 4 1 1 Etx BCC"
The CQ (FOX) message has no header

The program looks for Stx then stores data, therefore the BCC is preset to include the header characters.
When a message is received with BCC correct an ACK is sent to the TD

If SMALNK is set OK then message is converted to SCR3 protocol using a look-up table for the required berths

Message sent to SMA is repeated twice at 2sec intervals if ACK not received, thereafter SMALNK set at fail and Time Request sent at 10sec intervals

The data in the buffers consists of the last messages from the TD, if Base Scan required this data is used to update the SMA.

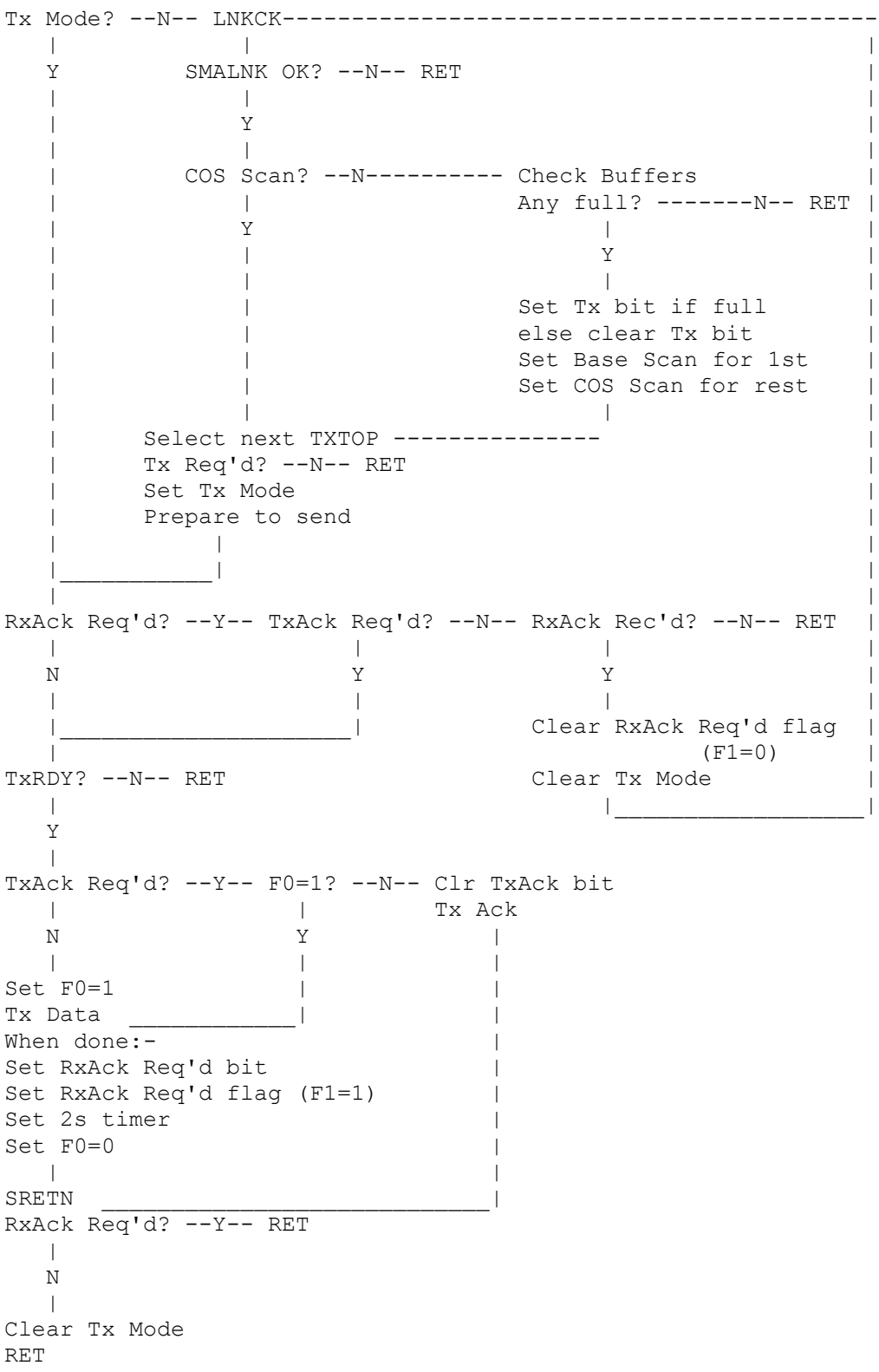
SOFTWARE NOTES

```
INIT   Preset 8243(2) ports 4,5,6 & 7
       Preset 8243(1) ports 4 & 5       LED1, LED2  lit.
       Program UART(1) 7 bits for TD
               UART(2) 8 bits for SMA
       Clear and preset various registers and RAM data
       Preset SMATX data to TIME REQUEST (STX FF ETX)
       Preset TXWRD (R6) for SMATX set (Bit6=1) and SMALNK fail (Bit5=0)
       Jump to STRT

PUART  Resets and programs a UART with the Mode Word stored in R5
       This allows for 7Bits (TD) or 8Bits (SMA)

STRT   Test for interrupt from TD or SMA
       Test TXWRD (R6) if Tx ACK required to TD
       Jump to SMATX for testing

TDLNK  Read data from TD
       If errors then clear TDSTATUS,reset reg'rs,set LED1 on and jump to
STRT
       If no errors set LED1 off
       Test for STX - YES - set TDSTATUS (R4=01)
                          - preset BCC (R2=08)
                    [Header SOH T R P S T R A H STX attached to each message]
                     - NO  - test for STX Rec'd

       STX REC'd ? - NO  - jump to STRT
                   - YES - data used for new BCC
                   - mask off bits 6&7 and store at R0 address
                   - test for ETX Rec'd
       ETX REC'D ? - YES - jump to FOXTST
                   - NO  - test for ETX
       If ETX then set TDSTATUS (R4=03)
       R0 and R3 (COUNT) decremented
       When R3=00 then R3=01 and R0=R0+1 for rest of message to allow the
         "FOX" message to be rec'd without storing it.

       FOXTST - test for "FOX" message - adjust BCC if yes as header is not
                attached to this message, clear R4 for CQTST
       Test BCC correct - set TXWRD (R6) Bit7=1 for ACK to TD if yes
                        - if no then return

       CQTST - test R4 Bit0 and return if not set else continue.
       Find IRN of the first berth in the message
       Test for "CA" - NO  - go to "CB" test
                   - YES - see if IRN valid - YES - load TD=SpSpSpSp in RAM
                                                  and increment R6 accordingly
                                                  then jump to ETXSET
                                                  - NO  - find "TO" berth IRN
       Test "TO" berth IRN valid - NO  - then return
                                 - YES - then set R0 at data start, call PACK
```

```
      ETXSET loads ETX in RAM, increments R6, loads 4LSB's of R6 to R2"
             Which is the SMA Tx counter and tests for CA message.
             If yes jumps to TOIRN else returns
      "CB" test - see if IRN valid - if no then return
                                   - if yes test for "CB" - if no "CC" test
                                   - if "CB" load TD=SpSpSpSP in RAM and
                                     increment R6 accordingly, go to ETXSET
      "CC" test - if yes then set R0 at data start, call PACK,go to FULLSET
                  if no then return

      FULLSET loads ETX in RAM, increments R6, loads 4LSB's of R6 to R2"
              Which is the SMA Tx counter and sets the "Berth Full" bit

TDTX  UART(1) tested for TxRDY=1 - if not then return to STRT
      When TxRDY set then ACK transmitted to TD
      Then reset TXWRD (R6) Bit7=0
PACK  R0 is set at data start, R1 is set at store address
      Converts 4 data bytes of a description to 3 bytes of packed data.
      The 2 MSB's have been stripped off each data byte before being stored
                   and are :-
                                                          X X 5a4a3a2a1a0a
                                                          X X 5b4b3b2b1b0b
                                                          X X 5c4c3c2c1c0c
                                                          X X 5d4d3d2d1d0d
      The 3 packed bytes are :-
                  5a4a3a2a1a0a5b4b; 3b2b1b0b5c4c3c2c; 1c0c5d4d3d2d1d0d

      Each packed byte is compared with the control characters STX,ETX,
      DLE,ACK & NAK and a DLE byte is added if the same
      R6 is incremented accordingly

FNDIRN Starting with R7=05, the last two characters of the berth name are
       compared with a look up table and R7 decremented until a match is
       found or R7=00
       Find next store buffer,set Tx Req'd Bit, STX, COS Scan Bit.
       The value of R7 is added to 30H to give the berth IRN, 30H was
       Chosen to avoid berth IRN's equating to a control character e.g.
       02=STX
       If R7=00 then result is invalid as no match was found
       Store berth IRN.

SMALNK Save R0 in SMATMP, R0 at SMASTATUS and UART(2) selected
       Read data from SMA
       If errors then clear SMASTATUS,set LED2 on,restore R0 and jump to
       STRT
       If no errors set LED2 off
       Test for ACK - if yes clear ACK Bit - TXSTATUS (R4") Bit7=0 then
       Return - if no then STXCK
       Test for STX - set SMASTATUS Bit7=1 if yes
                    - set BCC=00
       If STX rec'd - test for ETX rec'd - jump to SMA3 if yes
                    - if no - test for ETX - set SMASTATUS Bit6=1 if yes
                        - XOR data for new BCC then return
       If ETX rec'd (SMA3) - test BCC correct - return if no
       BCC correct - set TXSTATUS (R4") Bit0=1 for ACK to SMA
                     - set TXWRD Bit6=1 for SMA Tx & Bit5=1 for SMA OK
                     - set Bit4=0 to clear 80BIT
                     - restore R0 and jump to STRT
```

```
TIMER  Either 2sec or 10sec dependant on R5" preset to 01 or 05 after which
       jump to ACKCK
       ACKCK - test TXSTATUS (R4") Bit7=1 if ACK not rec'd - jump to NOACK
             - Bit7=0 - test TXWRD Bit5=1=SMA OK - YES - NEXT
                                                 - NO  - REPTRQ
       NEXT  - clear TXSTATUS, leave Bit0=1 if required (ACKTX)
       NOACK - if Bit6=0 - set Bit6=1 for 2nd transmission, set SMATX
               bit,F1=0
             - if Bit6=1 - set Bit5=1 for 3rd transmission, set SMATX
               bit,F1=0
             - if Bit5=1 - jump to TXFAIL
       REPTRQ - TXFAIL   - if Bit4=1 jump to TRQST
                           else set Bit4=1, preset 10s timer then return
       TRQST - set TXSTATUS to 80, leave Bit0=1 if required (ACKTX)
             - load Time Request message
             - clear SMAOK bit (TXWRD Bit5=0) & COS bit (Bit4=0)
             - set SMATX bit
             - clear F1
SMATX  UART(2) tested for TxRDY=1 - if not then return to STRT
       When TxRDY set - test R2" Bit7=1 - if yes then jump to BCC
                      - test TxACK req'd (R4"Bit0=1) - if yes jump to ACKTX
                      - set F1=1 for SMA Tx in progress
                      - XOR data for new BCC
                      - data transmitted to SMA
                      - counter decremented (R2") - if zero set Bit7=1
                      - test TxRDY=1 again for next byte
       BCC  - adjusted to remove STX
            - BCC transmitted to SMA
            - count (R2) recovered for repeat Tx if required
            - set ACK req'd bit - TXSTATUS (R4") Bit7=1
            - set registers for 2sec timer and start timer
            - set F1=0 for SMA Tx ended
            - if ACK Tx req'd then jump to STRT else clear SMATX bit
                                                    (TXWRD Bit6=0)
       ACKTX - if F1=1 then continue with SMA message
             - if F1=0 then ACK transmitted to SMA, clear ACKTX bit
               (R4"Bit0=0)
               also clear SMATX bit and jump to STRT
```

SMATX


Tx Mode? --N-- LNKCK
Y
SMALNK OK? --N-- RET
Y
COS Scan? --N---------- Check Buffers
Any full? -------N-- RET
Y
Set Tx bit if full
else clear Tx bit
Set Base Scan for 1st
Set COS Scan for rest
Select next TXTOP ---------------
Tx Req'd? --N-- RET
Set Tx Mode
Prepare to send
RxAck Req'd? --Y-- TxAck Req'd? --N-- RxAck Rec'd? --N-- RET
N
Y
Y
Clear RxAck Req'd flag
(F1=0)
TxRDY? --N-- RET
Clear Tx Mode
Y
TxAck Req'd? --Y-- F0=1? --N-- Clr TxAck bit
Tx Ack
N
Y
Set F0=1
Tx Data
When done:-
Set RxAck Req'd bit
Set RxAck Req'd flag (F1=1)
Set 2s timer
Set F0=0
SRETN
RxAck Req'd? --Y-- RET
N
Clear Tx Mode
RET

R.O.M. Code Dump

GLOSSARY AND INDEX OF TERMS

NOTE: In what follows "device" can refer to a card, module, or other system component according to context.

acknowledge - A control signal used to indicate to a device that an attempted communication has been successful.

address - The binary code used by the system to select a device. AK Shorthand for acknowledge.

alpha-numeric - A contraction of alphabetic-numeric. When applied to a device this term indicates that the device responds to, or generates, data which is to be interpreted as representing letters of the alphabet or numbers.

ASCII - American Standard Code for Information Interchange. - a code established by the American National Standards Institute to provide an agreed interpretation of transmitted binary data. The code is based on 7 bits.
In an 8 bit binary word, such as may be transmitted along a data bus, the 7 least significant bits (b0-b6) would, if ASCII is used, represent an agreed alpha-numeric character or control message. The 8th bit would be either ignored or interpreted as a parity bit. e.g. In ASCII, 1000001 represents the letter A and would appear on the data bus as 01000001.

asynchronous - Not synchronous. Synchronous communication between devices relies on the devices carrying out complimentary operations at the same time. Each device carries out a predetermined sequence of operations at a set rate and in a set order. The sequence must start and finish at the same time in both devices. Communication between synchronous devices relies on the receiving device being at the point in its sequence when it reads data in, at the same time as the transmitting device is at the point in its sequence when it outputs data. That is, the operation of the devices must be synchronised. In asynchronous communication the transmitting device is free to send data at any time. The start and end of each word in the message will be marked as specified by the transmission protocol. The receiving device will either respond to an interrupt generated by the incoming message, or test its receiving circuits for a message at intervals of less than the transmission time for the shortest possible message.

Backplane - The cards and modules of the system plug into edge connectors mounted in the card frame. The terminal pins of these connectors, which are accessible from the rear of the card frame, are known as the backplane.

backplane wiring - This is the wiring terminated on the pins of the edge connectors constituting the backplane. It includes both point to point wire wrapping and PCB or ribbon cable bussing, and connects together the devices which constitute the system.

baud rate - The rate at which information passes down a communication channel. In a serial transmission link the baud rate will correspond to the number of bits passing over the link in one second. However, the baud rate is not equivalent to bits per second. An 8 bit **parallel** link, operating at 1200 baud will pass 8x1200 (i.e. 9600) bits per second.

berth - The location in memory where a description is stored.

berth number - The number which the computer uses internally to identify a berth.

berth name - The name by which the berth is known to the signalman.

BICC-VERO - A manufacturer of racking systems.

binary - The system of counting to the base 2. In the decimal system we count to the base 10 and each of the digits can represent 10 numbers. e.g. In the decimal number "25" the LSD (least significant digit) "5" represents one of the ten possible "unit" numbers (0-9), and the MSD (most significant digit) "2" represents one of the ten possible "tens" numbers (0x10-9x10). Each increase in significance of a digit multiplies its value by ten. In the binary system, each digit can represent one of only two numbers (0 or 1), and each increase in significance of a digit multipies its value by two. Thus the decimal number 25 is equivalent to the binary number 11001.

i.e. binary	decimal
1	1
0x2	0
0x2x2	0
1x2x2x2	8
1x2x2x2x2	16
1 1 0 0 1	25

The number 25, which requires two digits to express it in decimal, requires five digits to express it in binary. However, binary has the advantage of being easy to represent electrically. - The two numbers of each digit can be represented by the two states of an electric circuit (ON and OFF). In practice, the circuit is switched to the potential of one of its (5V) power supply rails; 5V being taken to represent the condition of the binary digit represented above by 1, and 0V being taken to represent the condition of the binary digit represented above by 0.

The condition (1) represented by 5V is also referred to as **HIGH**: and the condition (0) represented by 0V is also referred to as **LOW**.

bit - Shorthand for **b**inary dig**it** - see **binary**.

BR 1810 - A specification issued by the D of S&T detailing the protocol to be followed in communications between electronic systems used by the S&T. - The purpose being to ensure compatibility and ease the assimilation of individual systems into any future Integrated Electronic Control Centre.

buffer - A circuit providing for the temporary storage of data passing between two devices. One of the devices will place the data in the buffer and set a control bit indicating that the buffer is full. The second device will test the control bit and, when appropriate, take the data from the buffer.

bus - You get on a bus to travel between areas of the town: data gets on a bus to travel between areas of the system. A bus is a group of conductors with a common purpose connecting together devices in the system. The conductors may be ribbon cable, wire wrap or PCB tracks. The bus will have associated conductors carrying signals which control access to the bus.

busbar - A heavy conductor used for distributing power to the system. Individual devices tap onto the busbar at any convenient point.

byte - The smallest block of data with which a computer (in this case the LR card) works. The microcomputer used has 8 bit buses for the passage of internal data; hence in this system a byte is a group of 8 bits. A byte is often referred to as a **word**.

carrier - A signal, at a fixed frequency, which is present on a MODEM communication link when no data is passing over the link (see **MODEM**).

CCITT - An international committee charged with establishing standards for data communication.

clock - A signal which controls the rate at which a circuit operates. Each time clock goes high (or low) the circuit is free to change state; clock goes alternately high and low at a fixed rate.

configuration - Cards used in ScR systems are designed with a considerable degree of flexibility. The cards can be combined in several ways to produce systems with differing capabilities, and some of the cards have circuit options built in to allow them to perform different tasks within the system. Once the system has been designed, the cards will have been combined in a particular way, and their role in the system, and hence their circuit options, will have been decided. - The circuit and cards are then said to be "configured" in a particular way. The combination of cards is known as the system configuration; and the circuit options chosen for the individual cards are known as the cards' configurations.

corruption - When the data in the system changes in a way not controlled by the programme, perhaps through power supply noise or radio interference, it is said to have been "corrupted". This phenomenon is known as corruption.

"D" - A type of multi-pin plug connector; so called because, when viewed head-on, the casing resembles the letter "D".

data - This is what it's all about! Data is what information is known as when it's inside a computer system. The job of the TD is to take information from the signalling system on the condition of tracks and routes and translate this to produce information on train movements for the operating staff. The translation process is known as data processing. - More specifically, the binary pattern of 1s and 0s within the system is the data. Data can be split into two catagories:

(a) **variable data** is obtained through the systems I/O circuits and changes as traffic conditions change.

(b) **fixed data** is placed in the system by the designer and only changes when the system is modified or extended (e.g. the look-up table in ROM relating the berth numbers to berth names).

DIL - **D**ual **I**n-**L**ine (**P**ackage). A form of packaging in which the component lead-out pins are arranged in two rows of pins set at a pitch of 0.1". In the most commonly used integrated circuit package these rows are set 0.3" apart.

DIP - See DIL.

DIN - The initials of the institute which sets the standards to which German electronic equipment must comply. As you might expect of the Germans, these standards are very comprehensive and widely complied with. The edge connectors and racking system we use are to the DIN standards; these being by far the wost widely adopted in this country for equipment of this nature.

duplex - The term used to describe a two-way transmission system. Simplex is transmission in one direction only between two devices: duplex is transmission in both directions between two devices. A full-duplex system is capable of transmitting in both directions at the same time: a half-duplex system must wait for transmission in one direction to stop before transmitting in the other direction. The system links are configured as 4 wire full-duplex systems. 2 wire full-duplex is possible, however we have chosen not to use it since fault-finding on the link then becomes rather difficult.

enable - To allow a circuit to operate. For example: If several cards are configured to place data onto a bus, only one must be allowed access at any given time. The bus buffer of the card which is to be allowed access is enabled by addressing the card through the routeing system. Enable is also the name of a signal performing such a function.

eurorack - The name in common use for racks to the DIN standard to which those used to contain the system are built.

event-driven - A system which is inactive unless an external occurrence requires it to operate is said to be event-driven.

fault - A hypothetical condition which ScR designed systems never enter.

FM - **F**requency **M**odulation. The method of encoding data on a carrier signal by altering its frequency.

full-duplex - see **duplex**.

handshaking - When two devices communicate, control signals are necessary to determine the sequence of data flow. That is, to determine in which direction the data is to pass, and, whether the device is ready to send or receive.

hardware - The physical components of the system.

header - The receptacle into which an insulation displacement connector plugs.

HIGH - see **binary**.

HP - The unit in which the width of a eurorack is measured, and hence, the unit in which the width of the components fitted to it are specified.

IC - **I**ntegrated **C**ircuit. A package containing part of the logic circuit. It will contain several logic gates, some of which can be tested individually, but all of which have to be replaced together due to the packaging. The ICs used in the system are usually "74 series" circuits, and the number printed on the package, following the series identifier, identifies the logic elements present in the circuit.

IDC - **I**nsulation **D**isplacement **C**onnector. A type of connector the electrical contact of which relies for its mechanical integrity on a system of twin blades which cut through the insulation around the conductor and bite into the conductor to establish an electrical connection.

IEC - Yet another standard. This one defines the connectors which we use for 110V.E

interface - As a noun: the junction between two devices or systems. As a verb: to link two devices or systems.

latch - A storage device into which data can be written and in which data will remain until cleared.

LED - Light Emitting Diode. A semiconductor which has the usual properties of a diode, but which in addition emits light of a fixed wavelength when forward biased.

LSB - **L**east **S**ignificant **B**it. In a binary code, the LSB is the digit with the lowest numerical significance (see **binary**).

LOW - see **binary**.

mark - see **MODEM**.

memory - The area of the computer in which is stored:

(a) the programme and

(b) the data

This memory is of two distinct types.

(i) ROM - Read Only Memory, the contents of which have been determined by the programmer and do not change even if the power is removed from the system. And

(ii) RAM - Random Access Memory, which would be known as RWM or Read/Write Memory if consonants were more readily pronounceable, the contents of which can be changed readily and which are determined by the operation of the programme. If the power is removed from the system the contents of RAM are lost. The system's ROM contains the programme and the fixed data. The system's RAM is used for data processing: i.e. it contains the variable data.

MSB - **M**ost **S**ignificant **B**it. In a binary code, the MSB is the digit with the highest numerical significance (see **binary**).

MOD - Shorthand for modification. This appears after the SES number identifying the card on some of the cards used in the system. It distinguishes small variations in the build characteristics of the card. The number following "MOD" identifies the exact variation. Cards with higher MOD numbers have extra facilities but are interchangeable with any card bearing the same SES number.

MODEM - **MOD**ulator/**DEM**odulator. A device used to transmit serial data over long distances in a comparatively interference-free form. It works by transmitting a fixed frequency known as the carrier when no data is present and shifting to one of two other frequencies (known as mark and space), one either side of the carrier frequency, to represent the two binary states of the data.

monostable - A circuit the output of which has one stable state. A control signal can change the state of the circuit for a fixed length of time, after which it returns to the stable state.

multiplexing - The process of combining data from many sources into a form suitable for transmission down a single channel.

NSB- ENFext ESFignificant EBFit. In a binary code, the digit next in numerical significance, either more or less, to one previously identified (see **LSB** & **MSB**).

opto-**isolator** - A device consisting of an LED and a photo-sensitive transistor encapsulated in a light-proof package. It is used to provide electrical isolation between two signals. One signal switches the light from the LED on and off, thus turning the photo-transistor on and off. The transistor controls the second signal and hence the first signal effectively controls the second without any electrical connection existing between the two.

oscillator - A device which produces a regular waveform: often used to provide a fixed frequency clock signal.

parity - A system of protecting against the acceptance of corrupt data by including an extra bit in each message. This bit is set high or low as appropriate to ensure that the binary sum of all the bits in the message (including parity) is always either odd (for odd parity) or even (for even parity). A transmission system operating with odd parity will reject any messages received with even parity (and vice-versa).

PCB - **P**rinted **C**ircuit **B**oard. A fibre-glass board carrying a pattern of copper tracking on its surface. This tracking forms the electrical connection between circuit elements.

populate - To fit the components to a board. Some of the boards in the system are designed such that they can be populated in more than one way: how they are to be used in the system decides how they are to be populated. The ASAD is one such board. The "population" of a board differs from the "configuration" of a board in that boards which have been populated differently have different components fitted and cannot function in each other's place; whereas boards which are configured differently have the same components present with optional links (which can of course be changed) determining how they are to be used.

port - A path in or out of the computer. In the ScR system usually a bi-directional buffer in which the data can be stored until the receiving device is ready to accept it.

processor - The part of the computer which does all the work. The processor takes each programme instruction in turn and carries out the logical operation required by that instruction, on the data specified by that instruction, before moving on to the next instruction.

programme - A list of instructions for the processor to carry out. The programmer's skill lies in picking the sequence of instructions which will produce the required results from the input data.

protocol - The rules governing communication between two devices or systems. The protocol will specify the handshaking, message format, baud rate etc.. It will be obvious that, to avoid the data being misinterpreted, the protocol must be strictly adhered to. Data which does not conform to the protocol will be ignored.

pulse - A short duration electrical signal. For example, a control signal will normally sit at one logic level (at which level it is said to be "inactive"). When it is required to fulfill its purpose it will move to the other logic level for a short period of time (when it is said to be "active"). This change in logic level is a pulse. The pulse will be specified by the direction of change in logic level (e.g. a negative going pulse changes from high to low and a positive going pulse changes from low to high), and by duration: i.e. the time spent in the active state.

RAM - **R**andom **A**ccess **M**emory (see **memory**).

RD - **R**ea**D**. A control pulse issued by one device to obtain data from another.

ribbon cable - A flat multi-core cable with the cores running parallel to each other at a fixed spacing in a single plane, with the insulation of each attached to that of its neighbours. This format makes the cable ideal for use with multi-way IDC systems.

ROM - **R**ead **O**nly **M**emory (see **memory**).

RS 232 - An internationally accepted communications interfacing standard, originating from America, based on a 3 wire communication channel with voltage polarity changes of the Rx and Tx wires (relative to the 3rd wire reference voltage) representing mark and space. RS232 also specifies the handshaking signals used and the pin allocations of the interfacing connector. V24 is essentially the same standard as defined by a -european- standards authority. The SES has adopted the convention of referring to RS 232 when the link under discussion uses the complete specification and to V24 when only the polarity changing principle has been used: This is incorrect usage but it does come in handy!

Rx - shorthand for receive.

ScR 3 - A specification detailing the protocol used for data transfer between electronic systems developed on the Scottish Region. This predates BR 1810, but remains in use since it is well established and can provide more efficient data transfer in certain applications.

SES - **S**ignalling **E**lectronics **S**ection. At the time of writing, the section in the Regional Signal Engineer's Office charged with responsibility for all of the S&T Dept.'s (non-telecom.) electronic systems.

simplex - One way data transmission (see **duplex**).

space - see MODEM.

tri-state - A type of logic, mainly used in circuits connected to a bus, which can assume, in addition to the binary logic levels, a third state which presents a high impedence to the bus; allowing other devices to use the bus without electrically stressing either circuit.

switch mode - A type of power supply in which the incoming mains voltage is first rectified, then used to power a high frequency invertor, the output of which is rectified and regulated to produce the required low voltage DC output. This method produces a compact and cost effective supply (the step-down transformer, now operating at high frequency, can be considerably smaller) and also has advantages in tolerance of mains fluctuations.

Tx - shorthand for transmit.

U - The unit in which the height of a eurorack is measured, and hence, the unit in which the height of the components fitted to it are specified. Note, however, that a 6U card is more than twice the height of a 3U card since it includes the height which, when two 3U racks are stacked, is occupied by the upper rail of the lower rack and the lower rail of the upper rack.

UART - **U**niversal **A**synchronous **R**eceiver **T**ransmitter. A communications IC designed to simplify the transmission and reception of serial data. In the multiplexing control card, the UART is acting as a transmitter. The microcomputer passes the data to be transmitted to the UART in parallel form. The UART adds the framing and parity bits required to form the complete message block, and passes the data to the MODEM in serial form. In the demultiplexing control card, the UART is acting as a receiver. The data arrives at the UART, from the MODEM, in serial form. The UART checks the framing and parity bits for errors and strips them from the data. The UART then informs the microcomputer of the arrival of the data and, when requested to, presents it, together with notification of any errors detected in parallel form. In short, the UART handles the time consuming tasks of serial transmission; freeing the microcomputer to perform other tasks.

V24 - see **RS232**.

varistor - A component which, below a set voltage, presents an extremely high resistance: above that voltage the resistance decreases rapidly. The effect of including this component in a parallel circuit is to "clamp" the voltage of the circuit slightly above the varistors set voltage.

wire-wrap - A system of wire termination which has largely replaced soldering in backplane wiring. The termination pins are square in cross-section with sharp edges. A special tool is used to wrap the wire tightly around the pin such that the edges of the pin bite into the wire; forming a firm electrical connection.

word - The smallest block of data representing a meaningful character. This often co-incides with a byte, but not always. For example, to transmit a description to the display units, 4 characters must be sent and hence 4 words are transmitted. However a modified 6 bit code (known as truncated ASCII) is used allowing the 4 characters to be represented by 24bits; hence the 4 words are transmitted as 3 bytes of data. (see also **byte**)

WR - **WR**ite. A control pulse used by a transmitting device to transfer data to a receiving device.

Line Routeing Card

SIGHTHILL PROTOCOL CONVERTER - RECORD OF MODIFICATION

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SIGHTHILL PROTOCOL CONVERTER - FAULT LOG

DATE	FAULT & ACTION TAKEN	TECHNICIAN