

N825126 AN

TRUTH TABLE FOR 256 x 4 BIPOLAR PROM (U32) 1K SEGMENT DECODE

Jumpers (HEX) Address (HEX) Output (HEX)	ROM 4 ROM 3 ROM 2 ROM 1				Jumpers (HEX) Address (HEX) Output (HEX)	ROM 4 ROM 3 ROM 2 ROM 1				Jumpers (HEX) Address (HEX) Output (HEX)	ROM 4 ROM 3 ROM 2 ROM 1			
	2	1	1	1		3	F	F	5		F	F	7	F
1 F F	1	1	1	1	3 F F			5 F F			7 F F			
1 E F					3 E F			5 E F			7 E F			
1 D F					3 D F			5 D F			7 D F			
1 C F	Column "1"				3 C F			5 C F			7 C F			
1 B F					3 B F			5 B F			7 B 7	0		
1 A F					3 A F			5 A F			7 A 7	0		
9 F					3 9 F			5 9 F			7 9 7	0		
1 8 F					3 8 F			5 8 F			7 8 7	0		
1 7 7	0				3 7 7	0		5 7 7	0		7 7 B	0		
1 6 7	0				3 6 7	0		5 6 7	0		7 6 B	0		
1 5 B		0			3 5 F			5 5 B	0		7 5 B	0		
1 4 B		0			3 4 F			5 4 B	0		7 4 B	0		
1 3 D			0		3 3 F			5 3 D		0	7 3 F			
1 2 D			0		3 2 B		0	5 2 D		0	7 2 F			
1 1 E				0	3 1 D		0	5 1 F			7 1 D		0	
1 0 E				0	3 0 E		0	5 0 E		0	7 0 E		0	
0 F F					2 C 7	0		4 F F			6 F F			
0 E F					2 E 7	0		4 E F			6 E F			
0 D F					2 D 7	0		4 D F			6 D F			
0 C F					2 C 7	0		4 C F			6 C F			
0 B F					2 B B		0	4 B F			6 B F			
0 A F					2 A B		0	4 A F			6 A F			
9 F					2 9 B		0	4 9 F			6 9 F			
0 8 F	Column "0"				2 8 B		0	4 8 F			6 8 F			
0 7 F					2 7 D		0	4 7 7	0		6 7 7	0		
0 6 F					2 6 D		0	4 6 7	0		6 6 7	0		
0 5 F					2 5 D		0	4 5 B	0		6 5 7	0		
0 4 F					2 4 D		0	4 4 B	0		6 4 7	0		
0 3 7	0				2 3 E		0	4 3 F			6 3 F			
0 2 B		0			2 2 E	Column "2"		0 4 2 F			6 2 B	0		
0 1 D			0		2 1 E			0 4 1 D		0	6 1 D		0	
0 0 E				0	2 0 E			0 4 0 E		0	6 0 E		0	

- NOTES:
1. Outputs are active Low
  2. A logic "1" is implied whenever there is no logic "0"
  3. Each grid line represents 1K of Z80 memory space

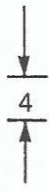


Figure 10

TRUTH TABLE FOR 256 x 4 BIPOLAR PROM (U32) 1K SEGMENT DECODE (Con't)

	Jumpers (HEX)			ROMs				Jumpers (HEX)			ROMs				Jumpers (HEX)			ROMs				
	Address (HEX)	Output (HEX)		ROM 4	ROM 3	ROM 2	ROM 1	Address (HEX)	Output (HEX)		ROM 4	ROM 3	ROM 2	ROM 1	Address (HEX)	Output (HEX)		ROM 4	ROM 3	ROM 2	ROM 1	
9	F	F						B	F	F					D	F	F					
9	E	F						B	E	F					D	E	F					
9	D	F						B	D	F					D	D	F					
9	C	F						B	C	F					D	C	F					
9	B	7	0					B	B	F					D	B	F					
9	A	7	0					B	A	F					D	A	F					
9	9	7	0					B	9	F					D	9	F					
9	8	7	0					B	8	F					D	8	F					
9	7	B		0				B	7	F					D	7	F					
9	6	B		0				B	6	F					D	6	F					
9	5	D			0			B	5	F					D	5	7	0				
9	4	D			0			B	4	7	0				D	4	B		0			
9	3	F						B	3	B		0			D	3	D			0		
9	2	F						B	2	D			0		D	2	D			0		
9	1	F						B	1	E				0	D	1	E				0	
9	0	E					0	B	0	E				0	D	0	E					0
8	F	7	0					A	F	F					C	F	F					
8	E	7	0					A	E	F					C	E	F					
8	D	7	0					A	D	F					C	D	F					
8	C	7	0					A	C	F					C	C	F					
8	B	B		0				A	B	7	0				C	B	F					
8	A	B		0				A	A	7	0				C	A	F					
8	9	B		0				A	9	7	0				C	9	F					
8	8	B		0				A	8	7	0				C	8	F					
8	7	D			0			A	7	B		0			C	7	F					
8	6	D			0			A	6	B		0			C	6	7	0				
8	5	D			0			A	5	B		0			C	5	B		0			
8	4	D			0			A	4	B		0			C	4	D			0		
8	3	F						A	3	D			0		C	3	E				0	
8	2	F						A	2	D			0		C	2	E				0	
8	1	F						A	1	F					C	1	E				0	
8	0	E					0	A	0	E				0	C	0	E					0

Unprogrammed Section

Figure 10 (Con't)



N82523AN

TRUTH TABLE OF

MK 6260  
(U31)

J	Address (Binary)				Address (Hex)	Output (Hex)	Outputs (Binary)									
	A <sub>15</sub>	A <sub>14</sub>	A <sub>13</sub>	A <sub>12</sub>			9	7	6	5	4	3	2	1		
1	1	1	1	1	1	F	F	B	2	1	1	1	1	0	1	1
1	1	1	1	0	1	E	E	7					0	1		
1	1	1	0	1	1	D	F	F								
1	1	1	0	0	1	C	F	F								
1	1	0	1	1	1	B	F	F								
1	1	0	1	0	1	A	F	F								
1	1	0	0	1	1	9	F	F								
1	1	0	0	0	1	8	F	F								
1	0	1	1	1	1	7	F	D						0		
1	0	1	1	0	1	6	F	D						0		
1	0	1	0	1	1	5	F	D						0		
1	0	1	0	0	1	4	F	C						0	0	
1	0	0	1	1	1	3	7	F	0							
1	0	0	1	0	1	2	B	F		0						
1	0	0	0	1	1	1	D	F			0					
1	0	0	0	0	1	0	E	F				0				
0	1	1	1	1	0	F	F	B						0		
0	1	1	1	0	0	E	F	7						0		
0	1	1	0	1	0	D	7	F	0							
0	1	1	0	0	0	C	B	F		0						
0	1	0	1	1	0	B	D	F			0					
0	1	0	1	0	0	A	F	E				0				
0	1	0	0	1	0	9	F	F								
0	1	0	0	0	0	8	F	F								
0	0	1	1	1	0	7	F	F								
0	0	1	1	0	0	6	F	F								
0	0	1	0	1	0	5	F	F								
0	0	1	0	0	0	4	F	F								
0	0	0	1	1	0	3	F	D						0		
0	0	0	1	0	0	2	F	D						0		
0	0	0	0	1	0	1	F	D						0		
0	0	0	0	0	0	0	F	C						0	0	

NOTES:

1. Outputs are active low
2. A logic "1" is implied wherever there is no logic "0".
3. Each grid line represents 4K of Z80 memory space.

65K with E5=1

65K with E5=0

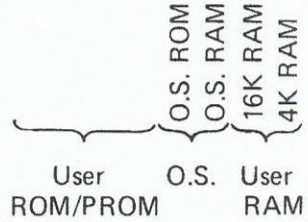
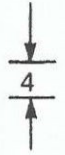


Figure 9

Offset(h)	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	
00000000	FC	FD	FD	FD	FF	FF	FF	FF	FF	FF	FE	DF	BF	7F	F7	FB	üýýýýýýýýýýýþß¿.÷û
00000010	EF	DF	BF	7F	FC	FD	FD	FD	FF	FF	FF	FF	FF	FF	E7	EB	ıß¿.üýýýýýýýýýçû