

# HM-6116/HM-6116L

## 2kx8

### static cmos ram

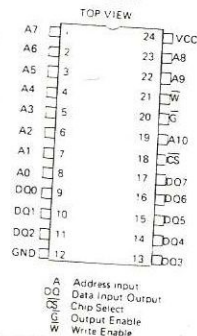
#### Features

- ASYNCHRONOUS
- FAST ACCESS : 120ns max
- STAND BY CURRENT : 100  $\mu$ A max
- OPERATING SUPPLY CURRENT : 70 mA max
- DATA RETENTION : 2 V min @ 50  $\mu$ A max
- STATIC MEMORY CELL
- INDUSTRY STANDARD PIN OUT
- HIGH OUTPUT DRIVE : 5std TTL load
- SINGLE SUPPLY : 5 V Vcc
- TTL COMPATIBLE INPUTS AND OUTPUTS
- WIDE TEMPERATURE RANGE

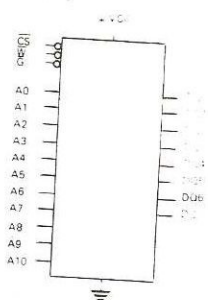
#### Description

- The HM 6116 is a 16384 bits static random access memory organized as 2048 words by 8 bits using C MOS technology and operates from the single 5V supply.
- The HM 6116 use "state of the art" MHS technology : the scaled self aligned junction isolation featuring low stand by current and fast address access time.
- The HM 6116 features fully static operation requiring no external clocks or timing strobes, equal access and cycle times.

#### Pinout



#### Logic Symbol

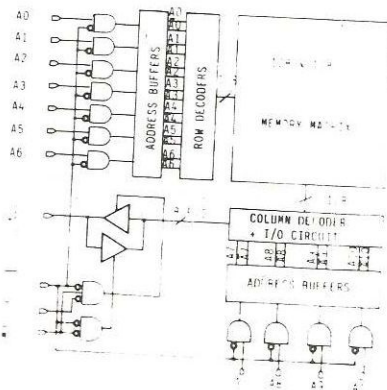


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#### Ordering Information

| DEVICE TYPE | PACKAGE     | TEMP. RANGE      |
|-------------|-------------|------------------|
| HM1-6116-5  | Ceramic DIL | 0°C to + 70°C    |
| HM3-6116-5  | Plastic DIL | 0°C to + 70°C    |
| HM1-6116L-5 | Ceramic DIL | 0°C to + 70°C    |
| HM3-6116L-5 | Plastic DIL | 0°C to + 70°C    |
| HM1-6116-2  | Ceramic DIL | -55°C to + 125°C |

#### Functional Diagram



# Specifications HM-6116-6116L

• ABSOLUTE MAXIMUM RATINGS :

Supply voltage (V<sub>CC</sub>-GND) : 0.3V to + 8.0V  
 Input or Output Voltage Applied (IGND : 0.3V)  
 to (V<sub>CC</sub> : 0.3V)  
 Storage temperature : -65°C + 150°C

• OPERATING RANGE

Military ( 2)  
 Commercial ( 5)

Operating Voltage Range

4.5V to 5.5V

Operating Temperature

-55° to + 125°

4.5V to 5.5V

0° to + 70°

## ELECTRICAL CHARACTERISTICS

### DC PARAMETERS

| SYMBOL           | PARAMETER                        | 6116<br>-5 | 6116<br>L-5 | 6116<br>-2 | UNIT | Value |
|------------------|----------------------------------|------------|-------------|------------|------|-------|
| ICCSB (1)        | standby supply current           | 15         | 12          | 20         | mA   | max   |
| ICCSB1 (2)       | standby supply current           | 2000       | 100         | 3000       | μA   | max   |
| ICCDR (3)        | data retention supply current    | 800        | 50          | 1200       | μA   | max   |
| ICOP (5)         | power supply current             | 70         | 70          | 85         | mA   | max   |
| ICC (4)          | average operating supply current | 70         | 70          | 85         | mA   | max   |
| VCCDR            | data retention supply voltage    | 2          | 2           | 2          | V    | min   |
| I <sub>I/O</sub> | input leakage current            | ± 2        | ± 2         | ± 2        | μA   | max   |
| VIL (6)          | input low voltage                | 0.8        | 0.8         | 0.8        | V    | max   |
| VIH (6)          | input high voltage               | 2.2        | 2.2         | VCC-2      | V    | min   |
| VOL (7)          | output low voltage               | 0.4        | 0.4         | 0.4        | V    | max   |
| VOH (7)          | output high voltage              | 2.4        | 2.4         | 2.4        | V    | min   |
| CI (8)           | input capacitance                | 8          | 8           | 8          | PF   | max   |
| CO (8)           | input-output capacitance         | 10         | 10          | 10         | PF   | max   |

NOTE 1  $\overline{CS} = VIH$

NOTE 2  $\overline{CS} = VCC-0.3V$

NOTE 3  $VCC = 2V$   $\overline{CS} \geq VCC-0.2V$

NOTE 4  $\overline{CS} = VIL$  ,  $I_{I/O} = 0$

NOTE 5 ICOP WITH A DUTY CYCLE = 100% ,  $I_{I/O} = 0$

NOTE 6  $VIL_{min} = 0.3V$  ,  $VIH_{max} = VCC + 0.3V$

NOTE 7  $I_{OL} = 4mA$  ,  $I_{OH} = 10mA$

NOTE 8 Capacitance sampled and guaranteed not 100% tested

Addresses and data inputs level  $\geq VCC-0.3V$

or :  $0.3V$  ,  $I_{I/O} = 0$

Addresses and data inputs level  $\geq VCC-0.2V$

or :  $0.2V$  ,  $I_{I/O} = 0$

Addresses and data inputs level =  $VCC$  or GND

$V_{I/O} = VCC$  or GND ;  $i_{I/O} = 0$

### AC PARAMETERS

#### WRITE CYCLE

| SYMBOL | PARAMETER (1)                        | 6116<br>-5 | 6116<br>L-5 | 6116<br>-2 | UNIT | Value |
|--------|--------------------------------------|------------|-------------|------------|------|-------|
| TAVAV  | write cycle time                     | 120        | 120         | 120        | ns   | min   |
| TELWH  | chip selection to end of write       | 70         | 70          | 70         | ns   | min   |
| TAVWH  | address valid to end of write        | 105        | 105         | 105        | ns   | min   |
| TAVWL  | address setup time                   | 20         | 20          | 20         | ns   | min   |
| TWLWH  | write pulse width                    | 70         | 70          | 70         | ns   | min   |
| TWHAU  | write recovery time                  | 5          | 5           | 5          | ns   | min   |
| TGHQZ  | output enable to output in high Z    | 40         | 40          | 40         | ns   | max   |
| TWLQZ  | write low to output in high Z        | 50         | 50          | 50         | ns   | max   |
| TDVWH  | input data valid to write high       | 35         | 35          | 35         | ns   | min   |
| TWHDX  | data hold from write time            | 5          | 5           | 5          | ns   | min   |
| TWHQX  | output active from end of write      | 5          | 5           | 5          | ns   | min   |
| TWLEH  | write low to chip select high        | -          | -           | -          | ns   | min   |
| TDVEH  | input data valid to chip select high | -          | -           | -          | ns   | min   |

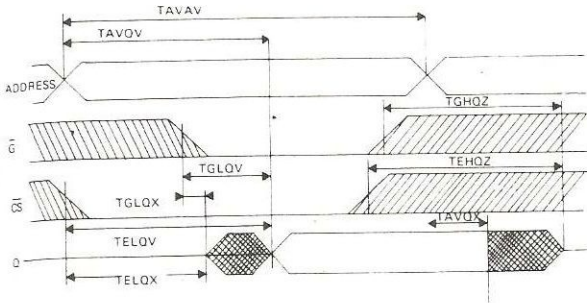
#### READ CYCLE

| SYMBOL | PARAMETER (1)                          | 6116<br>-5 | 6116<br>L-5 | 6116<br>-2 | UNIT | Value |
|--------|--|------------|-------------|------------|------|-------|
| TAVAV  | read cycle time                        | 120        | 120         | 120        | ns   | min   |
| TAVQV  | address access time                    | 120        | 120         | 120        | ns   | max   |
| TELQV  | chip select access time                | 120        | 120         | 120        | ns   | max   |
| TELQX  | chip select low to active output       | 10         | 10          | 10         | ns   | min   |
| TGLQV  | output enable to output valid time     | 80         | 80          | 80         | ns   | max   |
| TGLQX  | output enable to output in low Z time  | 10         | 10          | 10         | ns   | min   |
| TEHQZ  | chip select disable time               | 40         | 40          | 40         | ns   | max   |
| TGHQZ  | output enable to output in high Z time | 40         | 40          | 40         | ns   | max   |
| TAVQX  | output holdtime from address change    | 10         | 10          | 10         | ns   | min   |

NOTE 1 : LOAD : 100 pf (including JIG) AND TTL GATE

# Specifications HM-6116-6116L

## 1 READ CYCLE

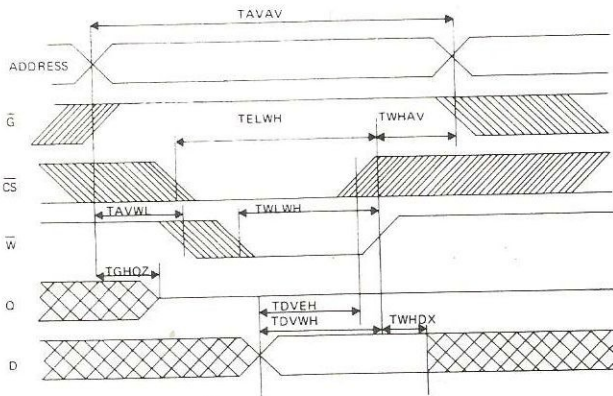


NOTE  $\bar{W}$  IS HIGH FOR A READ CYCLE

## TRUTH TABLE :

| CS | $\bar{G}$ | $\bar{W}$ | D     | Q     | POWER SUPPLY CURRENT | MODE  |
|----|-----------|-----------|-------|-------|----------------------|---|
| H  | X         | X         | Z     | Z     | ICCSB                | $\bar{CS} = V_{IH}$<br>DESELECT                 |
| H  | X         | X         | Z     | Z     | ICCSB1               | $\bar{CS} \rightarrow V_{cc} - 0.3$<br>DESELECT |
| L  | L         | H         | Z     | VALID | ICC                  | READ  |
| L  | H         | L         | VALID | Z     | ICC                  | WRITE   |
| L  | L         | L         | VALID | Z     | ICC                  | WRITE   |
| L  | H         | H         | Z     | Z     | ICC                  | DESELECT  |

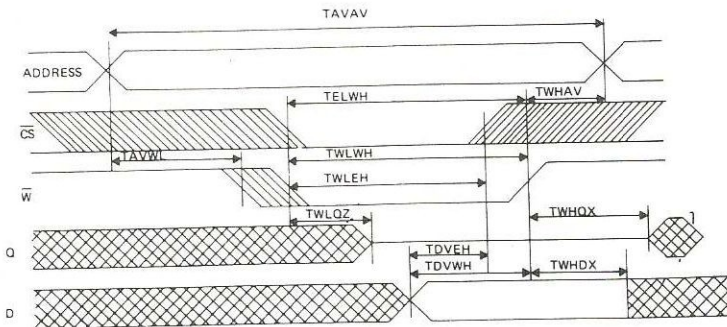
## 3 WRITE CYCLE TIME 1



This write cycle time is recommended for continuous writing.

$\bar{G} = V_{IH}$  during this write cycle.

## 3 WRITE CYCLE TIME 2



NOTE:  $\bar{G}$  IS LOW THROUGHOUT WRITE CYCLE.

This write cycle time may be used for write and read in the same cycle (write followed by read).

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