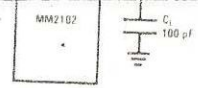
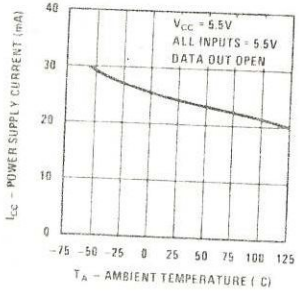


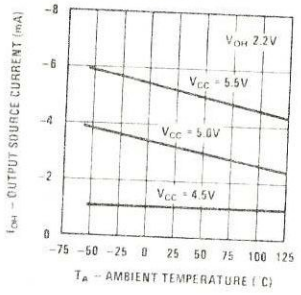
*Delay times measured at MM2102 output

typical performance characteristics

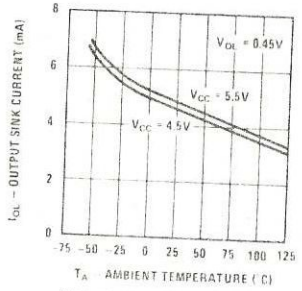
Power Supply Current vs Temperature



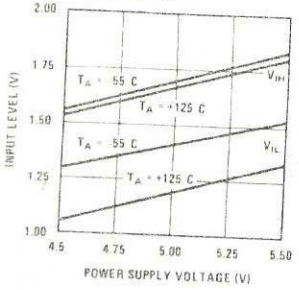
Output Source Current vs Temperature



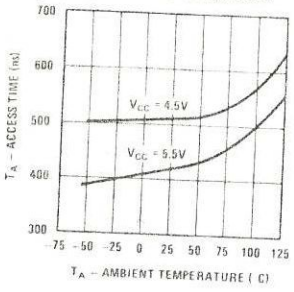
Output Sink Current vs Temperature



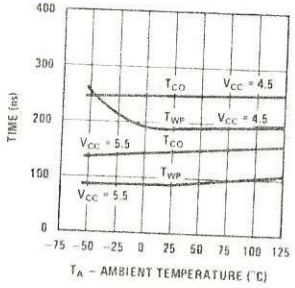
Input Levels vs Power Supply Voltage



Access Time vs Temperature



Write Pulse Width and Chip Enable–To Output Delay vs Temperature



MM2111, MM2111-1, MM2111-2 1024-bit (256 × 4) static MOS RAM with common I/O and output disable

general description

The National MM2111 is a 256 by 4 static random access memory element fabricated using N-channel enhancement mode Silicon Gate technology. Static storage cells eliminate the need for refresh and the peripheral circuitry associated with refresh. The data is read out nondestructively and has the same polarity as the input data. Common Data Input/Output pins are provided.

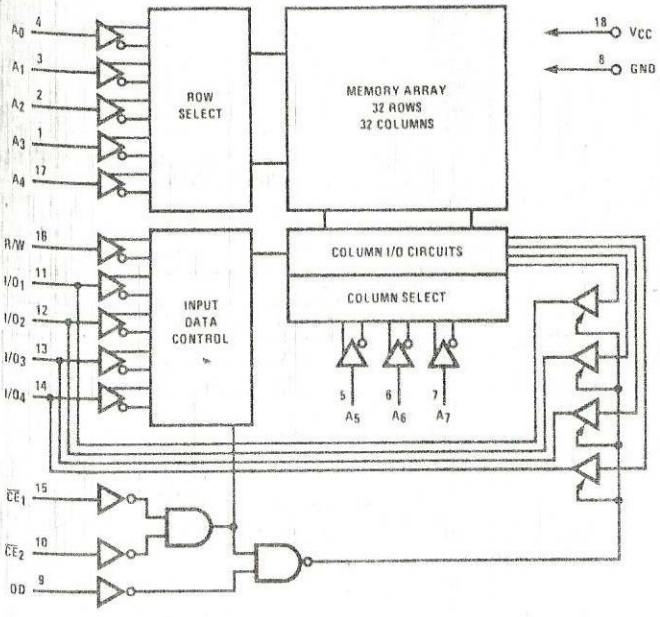
The 2111 is directly TTL in all respects: inputs, outputs and a single +5 V supply. The two Chip-enables allow easy selection of an individual package when outputs are OR-tied. The features of this memory device can be combined to make a low cost, high performance, and easy to manufacture memory system.

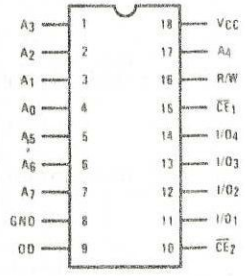
National's silicon gate technology provides excellent protection against contamination and permits the use of low cost Epoxy B packaging.

features

- Organization 256 Words by 4 Bits
- Common Data Input and Output
- Single +5 V Supply Voltage
- Directly TTL Compatible – All Inputs and Outputs
- Static MOS – No Clocks or Refreshing Required
- Access Time – 0.5 to 1.0 μs Max.
- Simple Memory Expansion – Chip Enable Input
- Low Cost Packaging – 18 Pin Epoxy B Dual-In-Line Configuration
- Low Power – Typically 150 mW
- Tri-State® Output – OR-Tie Capability

block and connection diagrams





PIN NAMES

A_0 A_7	ADDRESS INPUTS
OD	OUTPUT DISABLE
R/W	READ/WRITE INPUT
$\overline{CE}1$	CHIP ENABLE 1
$\overline{CE}2$	CHIP ENABLE 2
I/O_1 I/O_4	DATA INPUT/OUTPUT

Order Number MM2111D, MM2111-1D or MM2111-2D
See Package 4
Order Number MM2111N, MM2111-1N or MM2111-2N
See Package 16

Voltage On Any Pin With Respect to Ground	-0.5 V to +7 V
Power Dissipation	1 Watt

dc electrical characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5\ V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Current			10	μA	$V_{IN} = 0$ to 5.25 V
I_{LOH}	I/O Leakage Current[2]			15	μA	$\overline{CE} = 2.2\ V$, $V_{I/O} = 4.0\ V$
I_{LOL}	I/O Leakage Current[2]			-50	μA	$\overline{CE} = 2.2\ V$, $V_{I/O} = 0.45\ V$
I_{CC1}	Power Supply Current		30	60	mA	$V_{IN} = 5.25\ V$, $I_{I/O} = 0\ mA$, $T_A = 25°C$
I_{CC2}	Power Supply Current			70	mA	$V_{IN} = 5.25\ V$, $I_{I/O} = 0\ mA$, $T_A = 0°C$
V_{IL}	Input "Low" Voltage	-0.5		+0.65	V	
V_{IH}	Input "High" Voltage	2.2		V_{CC}	V	
V_{OL}	Output "Low" Voltage			+0.45	V	$I_{OL} = 2.0\ mA$
V_{OH}	Output "High" Voltage	2.2			V	$I_{OH} = -150\ \mu A$

Note 1: Typical values are for $T_A = 25°C$ and nominal supply voltage.

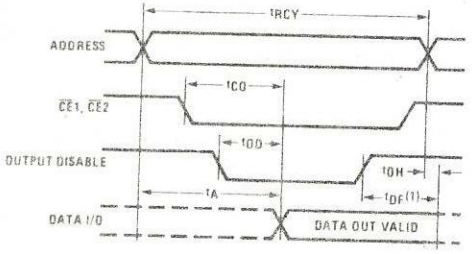
capacitance

$T_A = 25°C$, $f = 1\ MHz$

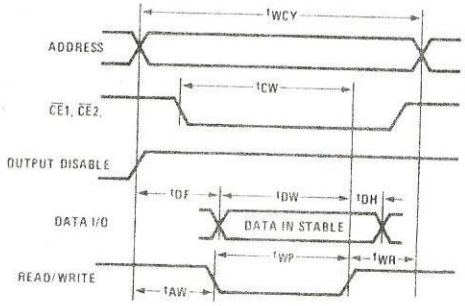
Symbol	Test	Limits (pF)	
		Typ.	Max.
C_{IN}	Input Capacitance (All Input Pins) $V_{IN} = 0\ V$	4	8
$C_{I/O}$	I/O Capacitance $V_{I/O} = 0\ V$	10	15

switching time waveforms

READ CYCLE (R/W = "1")



WRITE CYCLE



Note 1: t_{DF} is with respect to the trailing edge of $\overline{CE}1$, $\overline{CE}2$, or OD, whichever occurs first.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
READ CYCLE						
t_{RCY}	Read Cycle	1,000		1,000	ns	Input Pulse Levels: +0.65 to +2.2
t_A	Access Time			800	ns	Input Pulse Rise and Fall Times: 20 ns
t_{CO}	Chip Enable to Output			700	ns	Timing Measurement Reference Level: 1.5 V
t_{OD}	Output Disable to Output			200	ns	Output Load: 1 TTL Gate and $C_L = 100\ pF$
t_{DF}[1]	Data Output to High Z State	0				
t_{OH}	Previous Data Read Valid after change of Address	0			ns	
WRITE CYCLE						
t_{WCY}	Write Cycle	1,000			ns	Input Pulse Levels: +0.65 to +2.2
t_{AW}	Write Delay	150			ns	Input Pulse Rise and Fall Times: 20 ns
t_{CW}	Chip Enable to Write	900			ns	Timing Measurement Reference Level: 1.5 V
t_{DW}	Data Setup	700			ns	Output Load: 1 TTL Gate and $C_L = 100\ pF$
t_{DH}	Data Hold	100			ns	
t_{WP}	Write Pulse	750			ns	
t_{WR}	Write Recovery	50			ns	

MM2111-1 (500 ns Access Time)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
READ CYCLE						
t_{RCY}	Read Cycle	500		500	ns	Input Pulse Levels: +0.65 to +2
t_A	Access Time			350	ns	Input Pulse Rise and Fall Times 20 ns
t_{CO}	Chip Enable to Output			300	ns	Timing Measurement Reference Level: 1.5 V
t_{OD}	Output Disable to Output			150	ns	Output Load: 1 TTL Gate and $C_L = 100\ pF$
t_{DF}[1]	Data Output to High Z State	0				
t_{OH}	Previous Data Read Valid after change of Address	0			ns	
WRITE CYCLE						
t_{WCY}	Write Cycle	500			ns	Input Pulse Levels: +0.65 to +2
t_{AW}	Write Delay	100			ns	Input Pulse Rise and Fall Time 20 ns
t_{CW}	Chip Enable to Write	400			ns	Timing Measurement Referenc Level: 1.5 V
t_{DW}	Data Setup	280			ns	Output Load: 1 TTL Gate and $C_L = 100\ pF$
t_{DH}	Data Hold	100			ns	
t_{WP}	Write Pulse	300			ns	
t_{WR}	Write Recovery	50			ns	

MM2111-2 (650 ns Access Time)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
READ CYCLE						
t_{RCY}	Read Cycle	650		650	ns	Input Pulse Levels: +0.65 to
t_A	Access Time			400	ns	Input Pulse Rise and Fall Tim 20 ns
t_{CO}	Chip Enable to Output			350	ns	Timing Measurement Referen Level: 1.5 V
t_{OD}	Output Disable to Output			150	ns	Output Load: 1 TTL Gate an $C_L = 100\ pF$
t_{DF}[1]	Data Output to High Z State	0				
t_{OH}	Previous Data Read Valid after change of Address	0			ns	
WRITE CYCLE						
t_{WCY}	Write Cycle	650			ns	Input Pulse Levels: +0.65 to
t_{AW}	Write Delay	150			ns	Input Pulse Rise and Fall Tin 20 ns
t_{CW}	Chip Enable to Write	550			ns	Timing Measurement Refere Level: 1.5 V
t_{DW}	Data Setup	400			ns	Output Load: 1 TTL Gate a $C_L = 100\ pF$
t_{DH}	Data Hold	100			ns	
t_{WP}	Write Pulse	400			ns	
t_{WR}	Write Recovery	50			ns	