Autoranging frequency meter

This meter measures frequencies in four ranges up to 10MHz (9,999kHz) with automatic switching between the ranges. It displays the four most significant digits.

by F. P. Caracausi

The meter consists of four principal parts: input, timing, scaling and counter/display sections. Each is described separately but it must be noted that they are not necessarily separate modules, for example IC_{10} and IC_{11} are shared between the timing and scaling sections.

Counting and display

The main counter, Fig. 1, is built around a 74C926 i.c. which has four binary-coded decimal counters with multiplexed outputs to common-cathode led seven-segment displays. The counter module receives the signal to be counted through MCP. A positive signal (see note) on the MCP line, labelled 'store', will latch the counter value into the internal output latches and this value is displayed permanently as the display select input to the 74C926 is held low. The counter is cleared by a positive pulse on the MCL line and the 'carry out' signal is used to indicate an overflow, occurring whenever the count advances from 9999 to 0000. This negative-going transition is switched back to positive between 5999 and 6000. The underflow signal at MUF is a 1kHz (multiplexer frequency) pulse train which occurs as long as the most significant digit is zero; when the m.s.d. is not zero, there is no output.

Scaling

The signal to be measured is fed to three cascaded decimal dividers, $IC_{6,7,8}$ (Figure

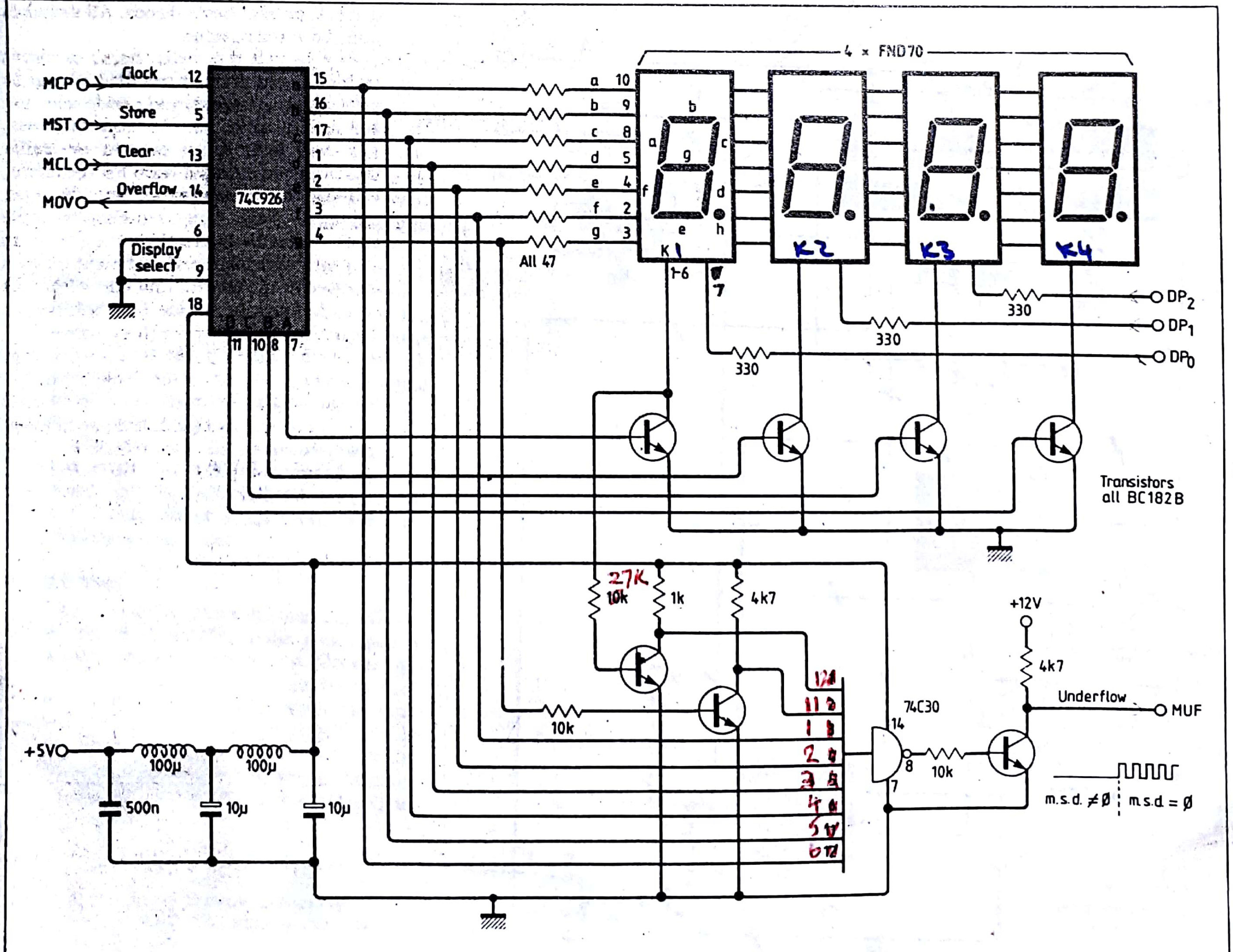

Fig. 1. *The counter and display module built around a 74C926 i.c.*

Fig 2. *The scaling circuit automatically selects the range to be displayed.* ▶

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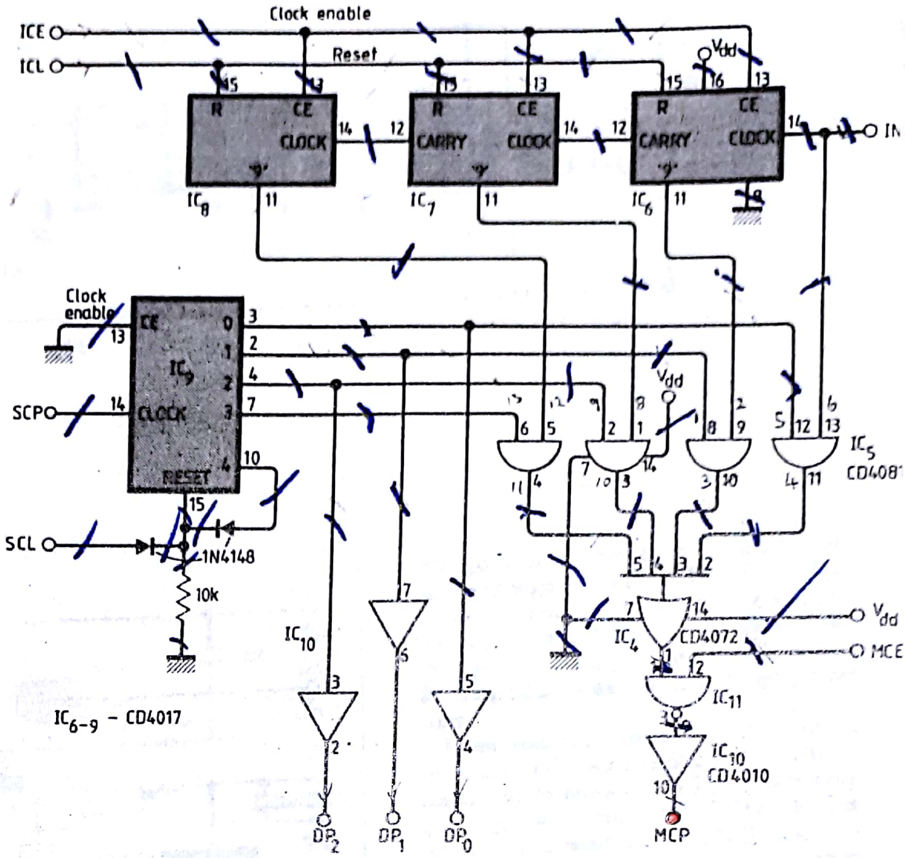

2). Depending on the value of the scale counter IC_9, the input frequency is divided by 1, 10, 100 or 1000. Provided that the MCE line is 'high', the signal is fed to the counter section through MCP, while the appropriate decimal point signal is sent through DP 0, 1 or 2. The displayed number is read as kHz.

Counter IC_9 is advanced by a positive clock pulse, SCP, and is cleared whenever it reaches a count of four or when the SCL signal is high. SCL and SCP both come from the counter module where SCP is generated when there is a overflow signal from the counter and SCL is derived from the underflow signal.

The counters $IC_{6,7,8}$ are enabled by a low signal on ICE and cleared by ICL going high. ICE and ICL are generated in the timing circuit when overflow or underflow signals occur.

Timing

The decimal counters IC_1 and IC_2 (figure 3), fed with a 50Hz pulse train, give a positive signal once a second. On the signal, MCE goes high which enables counter IC_3, disables $IC_{2,6,7,8}$, and stops the clock going to the main counter (signals MCE and MCP on the scaling circuit). MCE goes low if an overflow occurs on the main counter (MOV is low) and this makes Q on

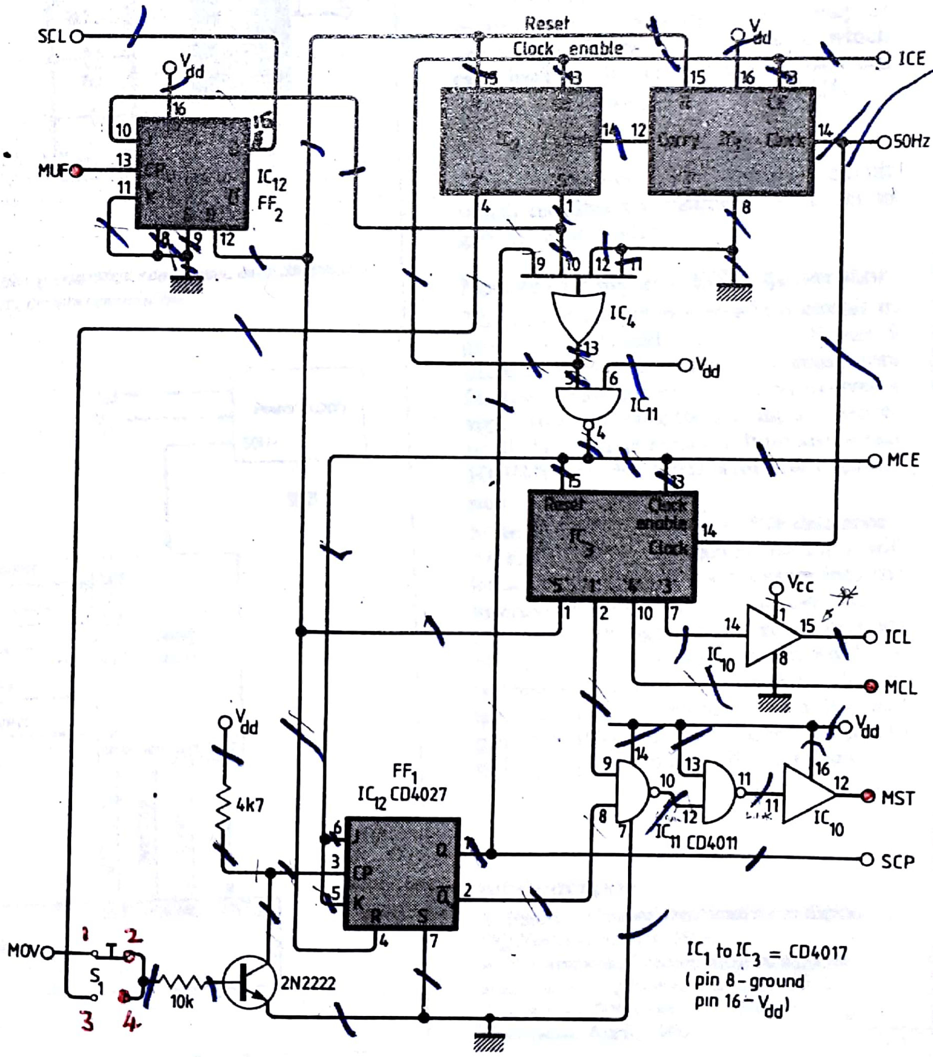

Fig 3. *The timing module generates control signals for the scaling and counting circuits.* ▶

* THIS SEEMS STRANGE +5V LOGIC GOING TO +12V LOGIC BUT WORKS OK

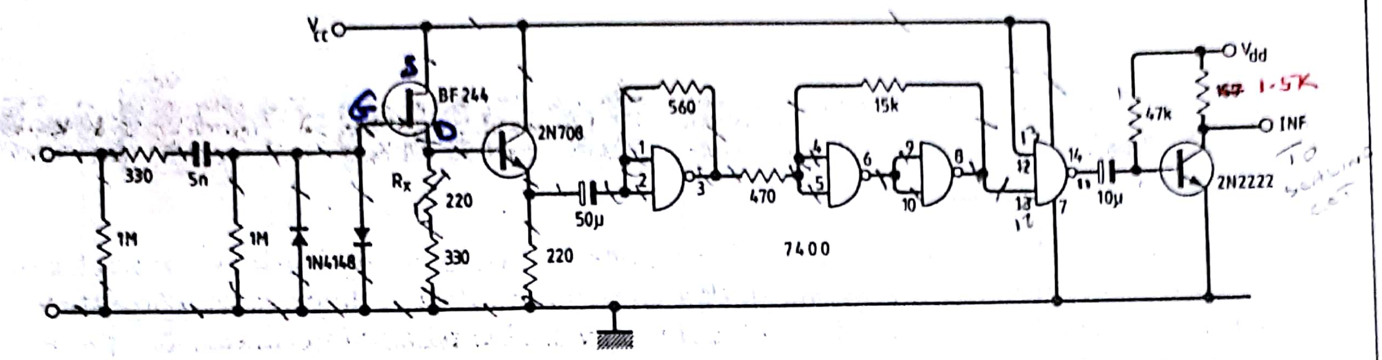

Fig. 4. *Input module.*

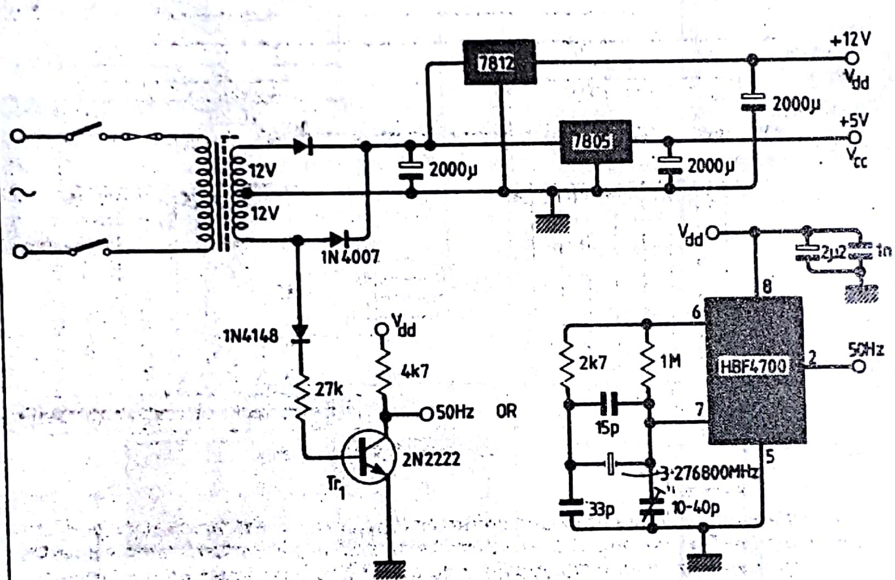

Fig. 5. *Power supply. Two versions of a 50Hz clock generator are given, one derived from the mains frequency, the other gives quartz crystal precision.*

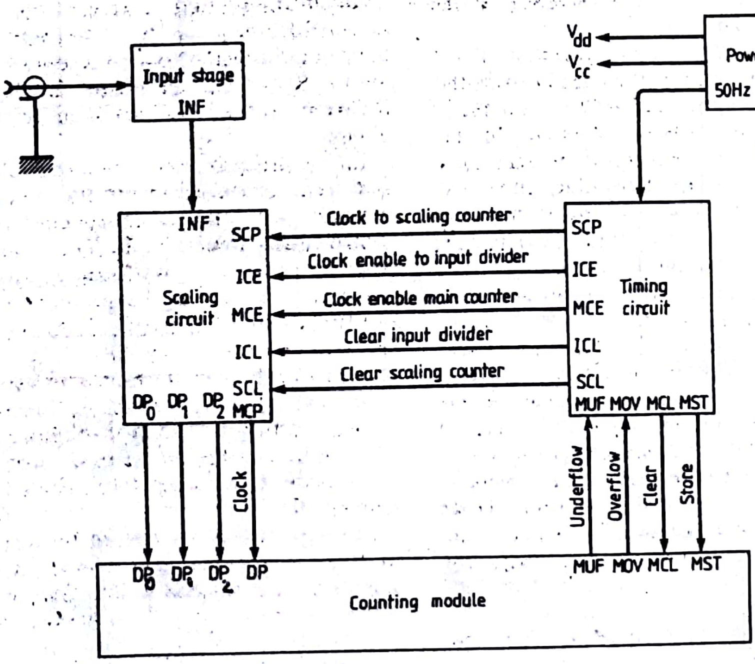

Fig. 6. *Interconnections between the sections.*

FF_1 go high and advances counter IC_9 by one to change the range. As IC_3 is enabled, it can generate the store signal, MST, and the clear signal, MCL. At the same time, through ICL, $IC_{6,7,8}$, both flip-flops and $IC_{1,2}$ are all reset and the next count period starts.

In an underflow condition FF_2 is set at the end of the count period as J on FF_2 is connected to output 5 of IC_2 which only goes high on a count of 50. When FF_2 is set, IC_9 is cleared through SCL and the next count starts at the lowest range (X.XXXkHz). An overflow condition may be simulated by pushing S_1. This may be necessary if the main counter locks, which can happen because the 74C926 can operate at frequencies up to 3 or 4MHz.

Input circuit

Figure 4 represents a classical circuit which requires no comment. R_x is set to give the best results.

Power supply and 50Hz generator

The power supply is a standard circuit to give V_{dd} (12V) and V_{cc} (5V). In Figure 5 there are two circuits for clock generators for the timing circuit. The first derives a signal from clipping the a.c. input, theoretically 50Hz. The second is built around an HBF4700 to give 50Hz with quartz precision.

Note. According to the 74C926 data sheet: "A low signal on the latch enable input will latch the number in the counters into the internal output latch". I found that it needed a high signal but if some versions of the i.c. work as described, it would be necessary to invert the signal by disconnecting the link between pin 11 of IC_{10} and pin 11 of IC_{11} and then connecting pin 11 of IC_{10} to pin 10 of IC_{11} (Figures 2 and 3).

Bibliography

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F. P. Caracausi, Frequenzimetro digitale automatico. CQ *Elettronica*, Sept. 1976
F. Bonadio, 50Hz con lo HBF4700A, *CQ Elettronica*, April, 1980.

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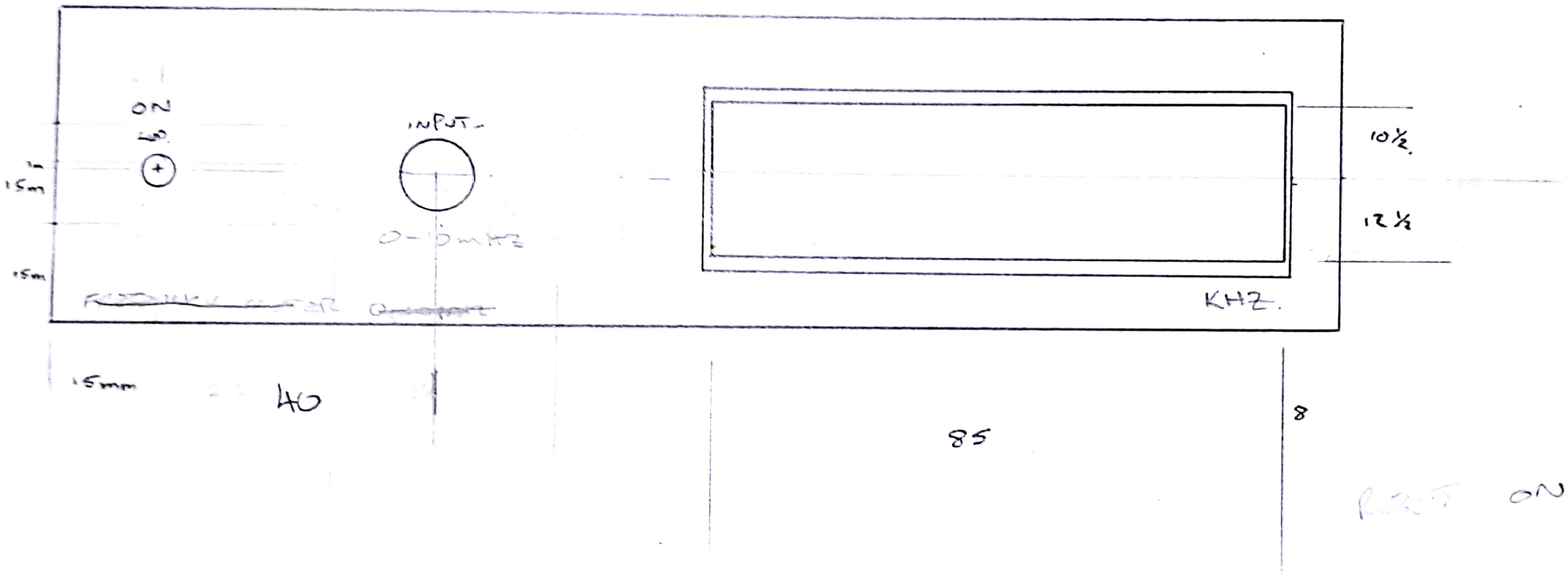

OFF/ON + PUSH SWITCH ON REAR PANEL.

FRONT PANEL.

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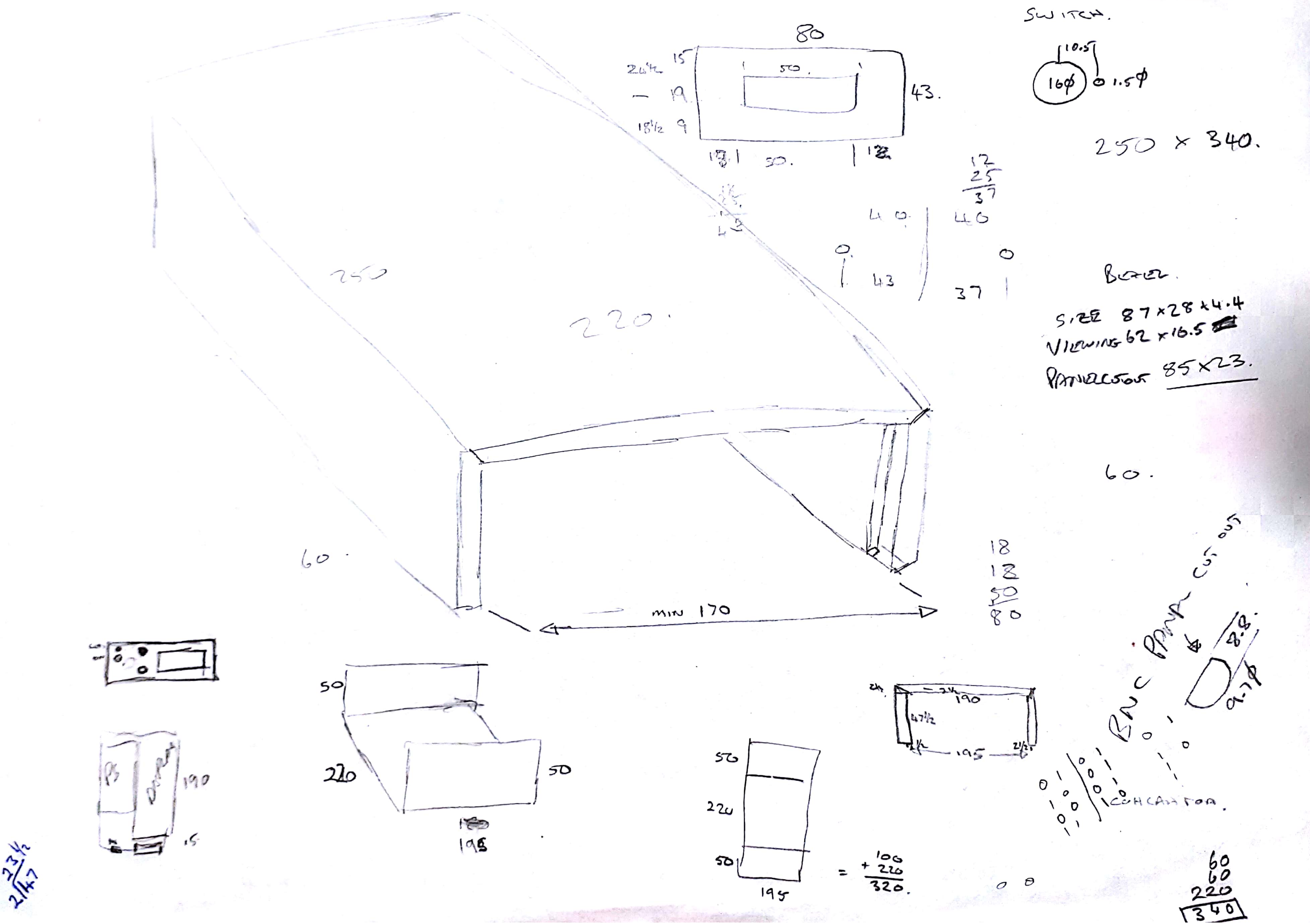

SWITCH.
10.5
16ϕ
1.5ϕ
250 x 340.
80
50
43.
24½ 15
19
18½ 9
50.
12
25
37
40.
40
43
37
BEZEL.
SIZE 87 x 28 x 4.4
VIEWING 62 x 16.5
PANEL CUTOUT 85 x 23.
60.
250
220.
60.
MIN 170
18
18
50
80
BNC PANEL CUT OUT
8.8.
9.7ϕ
CONCAVATOR.
60
60
220
340
50
220
50
195
190
B
DOPPLER
15
190
195
2½
4½
47½
56
220
50
195
= 100
+ 220
320.
23½
2/47